OPERATION AND MAINTENANCE MANUAL MODELS 6407 AND 6409 RF ANALYZER

WILTRON

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MANUAL ERRATA

MANUAL:
Title: 6400 Operation and Maintenance Manual, Models 6407 and 6409 RF Analyzer
Part Number: 10410-00043
Rev. Ltr/Date: E

ERRATA PACKET:
Part Number: 10901-00043

INSTRUCTIONS

1. Make all errata changes. Errata changes are listed in numerical order by page number.
2. Replacement pages are provided for all errata changes.

ERRATA 1, February 1990

1. **Page 6-2**
   Replace with enclosed pages 6-1 and 6-2, Changed: February 1990.

2. **Page 6-12**
   Replace with enclosed pages 6-11 and 6-12, Changed: February 1990.

SECTION VI
CALIBRATION

6-1 INTRODUCTION

This section contains 6407/6409 RF Analyzer calibration procedures, which are organized as follows:

Para.	Calibration
6-4	A4 Sweeper PCB
6-5	A3 Signal Channel PCB
6-6	CRT Set Up

Access to the instrument interior is gained by removing the four corner brackets and sliding the covers off (Figure 6-1).

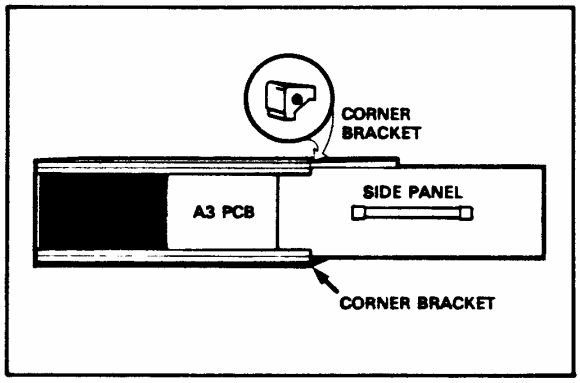

Figure 6-1. Gaining Access to RF Analyzer PCBs

6-2 RECOMMENDED TEST EQUIPMENT

The test equipment recommended for calibration of the 6407/6409 RF Analyzer is listed in Table 5-1.

6-3 ADJUSTMENTS FOLLOWING PCB REPLACEMENT.

Table 6-1 lists the required calibration following the replacement of PCBs.

6-4 A4 SWEEPER PCB ADJUSTMENTS

The A4 sweeper PCB is located on the bottom of the RF Analyzer beneath the RF deck. To make adjustments on this board, remove the bottom cover. Set the unit on its side so that you can access the adjusting pots on the board while also entering parameters from the control panel.

NOTE

The 6400 RF Analyzer cooling system is designed to operate with the covers on. If you are working in a warm environment with the covers off, it is possible that the current-limiting polyswitches on the power supply board (A9) could

Table 6-1. Recommended Adjustments Following PCB Replacement

If the Following PCB Was Replaced:	Perform the Following Adjustments in Section(s):
A3 PCB	6-5.1, 6-5.2
A4 PCB	6-4.1, 6-4.2, 6-4.3, 6-4.4

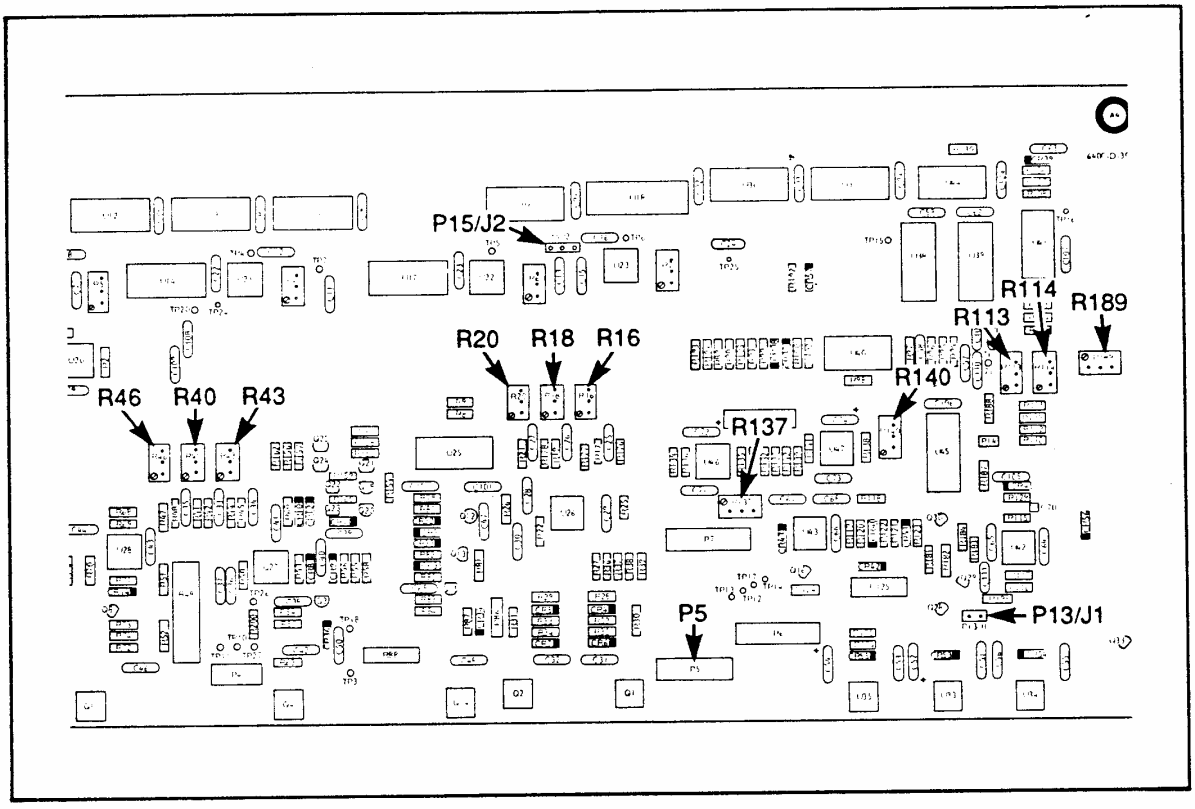

Figure 6-2. Locations of A4 PCB Adjustments

trip, which would limit power to the circuits. This is not an instrument failure, but merely a protective action built into the instrument. If this occurs, turn the instrument OFF and allow it to cool before proceeding with the calibration.

The A4 PCB adjustment pots referenced in the text are called out in Figure 6-2.

NOTE

A4R177 and A4R200 are select on test resistors and may have to be changed after replacing the YIG driver or A4 PCB.

1. Set the center frequency to 100 MHz, the width to 0 MHz, the source power to 2 dBm, and the smoothing to MIN.

2. Connect a counter to the 6400 RF output and adjust A4R46 for a counter reading of 100 MHz ±100 KHz. The frequency should jump in multiples of 25 MHz and a positive increase in frequency should correspond to a clockwise rotation of A4R46. If it is not possible to achieve 100 MHz, reselect A4R200 for either a higher or lower value.

NOTE

If the range on A4R18 is insufficient when performing the FM coil calibration, it may be necessary to change A4R177 to either 10k or 20k. The nominal value is 15k.

(d) Press Channel A menu, and ensure that the menu cursor highlighs SET MEASUREMENT TYPE.
(e) Press SELECT.
(f) Move the menu cursor to highlight POWER dBm, then press SELECT.
(g) Set the Power Level to 0.0 dBm (+0.1 dBm without the optional attenuator).
(h) Press the Channel A menu key and move the menu cursor to highlight SET TEST LIMITS.
(i) Press SELECT, then set Low Limit to -20 dB.
(j) Press the MARKERS key and ensure that the menu cursor highlights M1.
(k) Press ENTER to activate M1.
(l) Using the analog knob (spinwheel), set marker M1 to where the filter skirt intersects the -20 dBm limit line. Note this M1 frequency.

3. On the A3 PCB, adjust R71 fully clockwise.

4. On the RF Analyzer:
(a) Press SOURCE FREQUENCY, WIDTH and enter 25 MHz.
(b) Press SOURCE FREQUENCY, CENTER and enter the value noted in step 2.(1).
(c) Set Resolution to 5.0 dB.
(d) Press the SOURCE FREQUENCY, CENTER key, then use the analog knob (spinwheel) to position the filter skirt notch at center screen.
(e) Set Offset to -20 dB.
(f) Using the analog knob (spinwheel), increase the RESOLUTION to 0.2 dB, while readjusting the OFFSET, as necessary, to keep the filter skirt notch displayed at center screen.

5. Adjust R71 to obtain a smooth trace. The range change should be visible as R71 is adjusted (Figure 6-10).

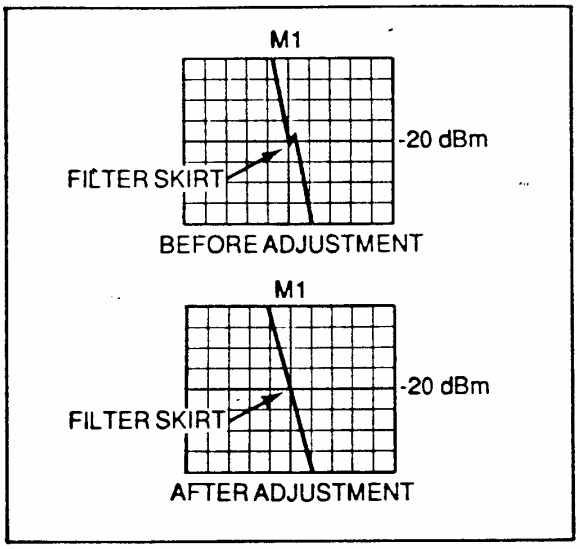

Figure 6-10. R71 Adjustment: Before and After.

6-5.2 Overall Gain Calibration

1. On the power meter:
(a) Zero and calibrate the power meter.
(b) Set the correct CAL factor as indicated on the power meter head for 50 MHz.

2. Disconnect the detector from the RF Analyzer, then remove the filter.

3. On the RF Analyzer:
(a) Press RESET then SELECT.
(b) Set a CW frequency of 50 MHz.
(c) Switch Channels A and B OFF.
(d) Set the power level to 0.1 dBm.
(e) Set smoothing to MIN.
(f) Press the Channel A MENU key and ensure that SET MEASUREMENT TYPE is highlighted on the menu display.
(g) Press SELECT.
(h) Move the menu cursor to highlight (or select) POWER dBm, then press SELECT.

3. Connect the power meter as shown in Figure 6-11.

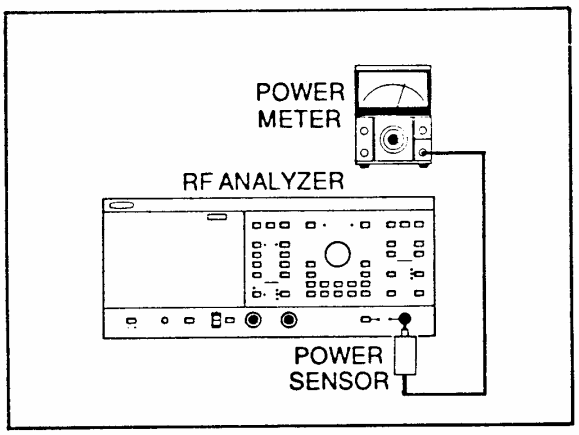

Figure 6-11. Overall Gain Calibration Test Setup

4. Ensure that Channel A is OFF.

5. Adjust the power level of the RF Analyzer until a reading of +0.1 dBm ±0.1 dB is obtained on the power meter.

6. Disconnect the power meter from the RF Analyzer.

7. Connect the Detector to Channel A and to the RF Analyzer output.

8. On the RF Analyzer:
   (a) Turn Channel A ON.
   (b) Press the MARKERS key and ensure that the M1 is highlighted on the menu display.
   (c) Enter an M1 value of 50 MHz.

9. On the A3 board, adjust R38 until the marker readout is the same as that set in step 5 to within ±0.02 dB.

10. Perform the following steps in the exact order listed:
    (a) With Channel A ON, remove the detector that is plugged into the Channel A input on the control panel.
    (b) Ensure that Channel B is OFF, then turn Channel A OFF.
    (c) Reconnect the detector to the Channel A input and turn Channel A ON.
    (d) Press the MARKERS key and note the marker readout (frequency); repeat step 9 as necessary.
    (e) Connect the detector input cable to Channel B.
    (f) Turn Channel B ON. Ensure that the LED beside Channel B flashes.
    (g) Press the Channel B menu key.
    (h) Move the menu cursor to highlight, or select, SET MEASUREMENT TYPE, then press SELECT.
    (i) When the next menu appears, move the cursor to highlight POWER dBm, then press SELECT.

11. Press the MARKERS key to display the marker readout; record this marker readout: _____ dBm.

12. Ensure that the marker frequency is set to 50 MHz
    (a) Adjust R76 1/4 turn in either direction.
    (b) Disconnect the detector while channel B is still ON.
    (c) Turn channel B OFF.
    (d) Reconnect the detector to channel B.
    (e) Turn channel B back ON (LED will flash).

13. Turn the marker back ON.

14. Observe the marker readout again. Repeat step 12 until the reading is within ±0.02 dB of the value recorded in step 11.

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GENERAL INFORMATION

SECTION I
GENERAL INFORMATION

1-1 SCOPE OF THE MANUAL

This manual provides general, installation, and operation information for the Models 6407 and 6409 RF Analyzer (Figure 1-1).

1-2 INTRODUCTION

Section I provides information about the equipment identification number, performance specifications, and options.

1-3 IDENTIFICATION NUMBER

All WILTRON instruments are assigned a six-digit ID number, such as "505001." This number appears on a decal affixed to the rear panel. Please use this identification number in any future correspondence with WILTRON Customer Service about this instrument.

1-4 DESCRIPTION OF 6400 SYSTEM

The 6407 and 6409 RF Analyzers are complete measurement systems for testing RF components and systems. Each consists of an RF analyzer, with its own built-in scalar network analyzer and sweep-frequency source, an external RF detector, and an SWR Autotester. The RF detector is used to measure transmission loss and absolute power, and the SWR Autotester is used to measure return loss.

1-5 OPTIONS

The following options are available:

Option 1, Rack Mount. A kit is available containing mounting brackets and chassis track slides. The track slides have a 90-degree tilt capability.

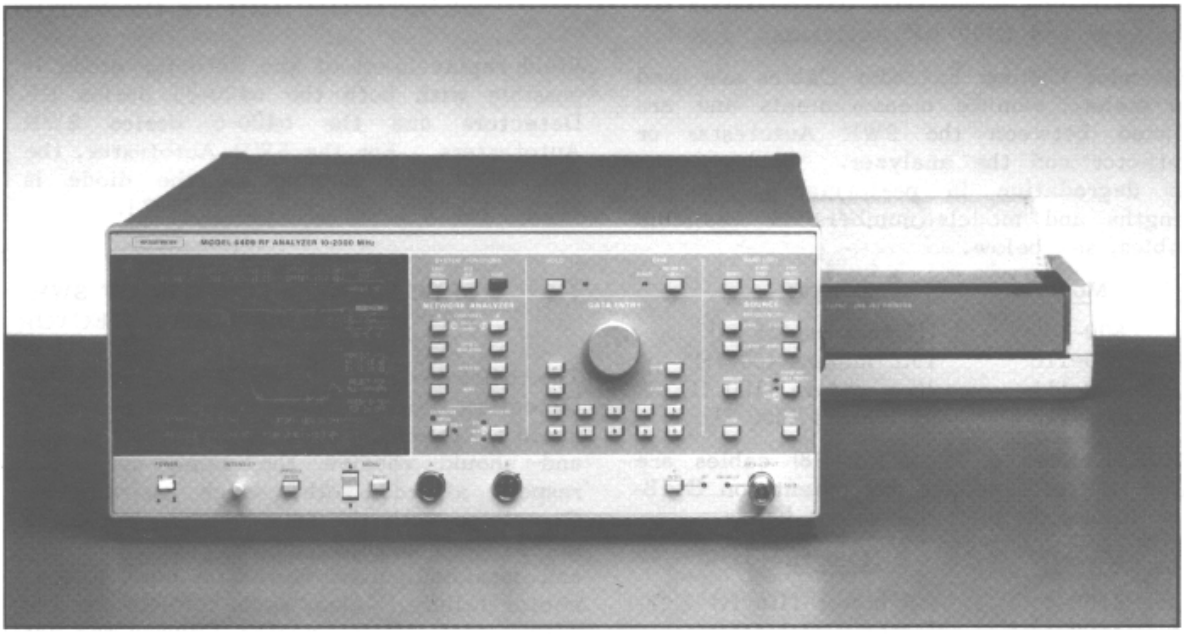


Figure 1-1. Model 6409 RF Analyzer and 2225C Ink Jet Printer

Option 2, 70 dB Step Attenuator, 10 dB Steps. RF Analyzer comes supplied with a control-panel- or GPIB-programmable 10 dB step attenuator having a 70 dB range.

Option 3, GPIB Interface. RF Analyzer is equipped to operate on the IEEE-488 Interface Bus. With Option 3 installed, all control-panel keys, except line POWER, are bus-programmable. Option 3 may be installed in the field.

Option 4, 75-Ohm RF Output (6407 only). RF Analyzer comes supplied with an RF OUTPUT connector having an impedance of 75 ohms.

Option 5, Graphics Printer. RF Analyzer is supplied with a Model 2225C Inkjet Printer, 2225-1 Interface Cable, one 2225-2 Inkjet Cartridge, and 500 sheets of 2225-3 Fan Fold Printer Paper.

Option 6, Protective Cover. RF Analyzer comes with a protective cover for the control (front) panel.

1-6 ACCESSORIES

The following accessories are available for the 6407 and 6409 RF Analyzers:

Extender Cables: Extender Cables are used to make remote measurements and are placed between the SWR Autotester or detector and the analyzer. Cables cause no degradation in performance. For lengths and models numbers of available cables, see below.

Model	Length
800-109	7.6 meters (25 ft)
800-110	15.2 meters (50 ft)
800-111	30.4 meters (100 ft)
800-112	61 meters (200 ft)

GPIB Cables: GPIB (IEEE-488) cables are used to interconnect instruments on GPIB. See listing of available cables below.

Model	Length
2100-5	0.5 meter (1.6 ft)
2100-1	1 meter (3.3 ft)
2100-2	2 meters (6.6 ft)
2100-4	4 meters (13.2 ft)

RF Limiters: RF limiters are used to protect 6400 detectors against damage from:

- DC Voltage--blocks up to 50 volts
- AC Voltage--filters 60 hertz and below signals up to 100 volts and impulse currents up to 500 milliamperes
- RF Power--protects for up to 4 watts from 1 to 1500 megahertz.

See listing of available RF limiters below.

Model	Connectors	Impedance (Ohms)
1B50	BNC Male & Female	50
1N50	N Male & Female	50
1B75	BNC Male & Female	75
1N75	N Male & Female	75

1-7 SPECIFICATIONS

Specifications for the 6407 and 6409 RF Analyzers and the 6400 SWR Autotesters and RF Detectors are provided in Table 1-1 on page 1-4.

1-8 REPLACEMENT DIODE FOR SWR AUTOTESTER AND RF DETECTOR

Field replacement of the detector diode is possible with both the 6400-71 Series RF Detectors and the 6400-6 Series SWR Autotesters. For the SWR Autotester, the WILTRON part number of the diode is 10-9. For the detector, it is 10-21.

1-9 PRECAUTIONS FOR USE OF SWR AUTOTESTER AND RF DETECTOR

The 6400-Series SWR Autotesters and RF Detectors (RF components) are high-quality, precision laboratory instruments and should receive the same care and respect afforded other such instruments. Complying with the following precautionary notes will guarantee longer component life and less equipment downtime due to connector failure. Also, such compliance will ensure that RF component failures are not due to misuse or abuse--two failure causes not covered under the WILTRON warranty.

a. Beware of Destructive Pin Depth on Mating Connectors. Measure the pin depth (Figure 1-2) of the connector that mates with the RF component before mating. Based on RF components returned for repair, destructive pin depth on mating connectors is the major cause of failure in the field. When an RF component connector is mated with a connector having a destructive pin depth, damage will likely occur to the RF component connector. (A destructive pin depth has a center pin that is too long in respect to the connector's reference plane.)

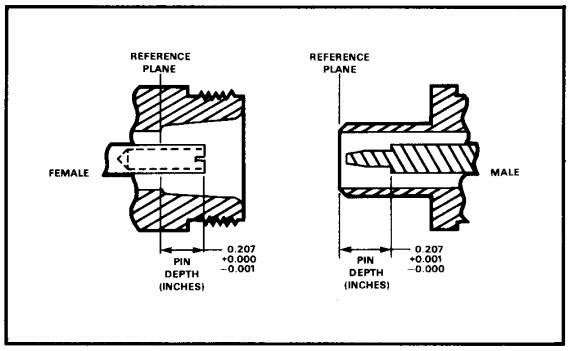


Figure 1-2. Reading N-Connector Pin Depth

The center pin on an RF component connector has a precision tolerance measured in mils (1/1000 inch). Whereas, connectors on test devices that mate with RF components may not be precision types, and their pins may not have the proper depth. Consequently, they must be measured before mating to ensure suitability. When gauging pin depth, if the test device connector measures out of tolerance (Table 1-2) in the "+" region (Figure 1-3) the center pin is too long. Mating under this condition will probably damage the RF component connector. On the other hand, if the test device connector measures out of tolerance in the "-" region, the center pin is too short. A mating, while not causing any damage, will now result in a poor connection and a consequent degradation in performance.

Table 1-2. RF Component Pin-Depth Tolerance

TEST PORT CONNECTOR TYPE	PIN DEPTH (MILS)	MMC GAUGE* READING
N-male	207 $^{+0.003}_{-0.000}$	210 $^{+0.003}_{-0.000}$
N-female	207 $^{-0.003}_{+0.000}$	same as pin depth

*MMC is Maury Microwave Corp.

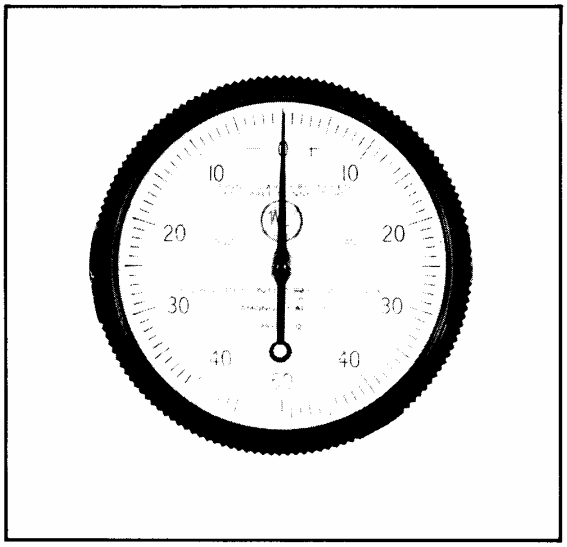


Figure 1-3. MMC Pin Depth Gauge

b. Avoid Over-Torquing Connectors. Over-torquing connectors is destructive; it may damage the connector center pin. Finger-tight is usually sufficient, especially on type N connectors. NEVER USE PLIERS TO TIGHTEN CONNECTORS

c. Do Not Disturb Teflon Tuning Washers on Connector Center Pins. The center conductor on most RF component connectors contains a small teflon tuning washer located near the point of mating (interface). This washer compensates for minor impedance disconti-

nuities at the interface. The washer's location is critical to the RF component's performance, DO NOT DISTURB.

d. Avoid Mechanical Shock. RF components are designed to withstand years of normal bench handling. However, do not drop or otherwise roughly treat them. They are laboratory-quality devices, and like other such devices, they require careful handling.

e. Keep Connectors Clean. The precise geometry that makes possible the RF component's high performance can be easily disturbed by dirt and other contamination adhering to connector interfaces. When not in use, keep the connectors covered.

Table 1-1. Specifications

Source

Frequency Range:
6407: 1 to 1000 MHz
6409: 10 to 2000 MHz
Frequency Resolution: 10 kHz
Frequency Accuracy: ±100 kHz
Frequency Drift:
With Time: <100 kHz/hour
With Temperature: 25 kHz/°C
With 10% Change in Line Voltage: <100 kHz
With 3:1 Load SWR: <200 kHz
Leveled Output Power Range: +12 dBm to 0.1 dBm in 0.1 dB steps
With Optional Attenuator: +10 dBm to -69.9 dBm in 0.1 dB steps
RF Output Impedance: 50 ohms
(Optional 75 ohms is available on 6407)
Leveled Power Output, 75 Ohm Version:
Without Optional Attenuator: +10 dBm
With Optional Attenuator: +8 dBm
RF Output Connector: Type N Female
Source Match: <1.5 SWR
Output Power Flatness: ±0.3 dB
With Attenuator: ±1.0 dB (6407 with Option 4, ±0.5 dB), plus 0.1 dB/10 dB of attenuation
Signal Purity:
Harmonics: <-30 dBc
(except -25 dBc on the 6407 between 1 and 2 MHz.)
Non-Harmonic Spurious: <-40 dBc
Residual AM: <-50 dBc in 100 kHz BW
Residual FM: <5 kHz peak, 30 Hz to 15 kHz post-detection Bandwidth
Sweep Time: Determined automatically by number of data points and amount of smoothing selected.

Number of Data Points	Smoothing	Typical Sweep Time
101	OFF	<100 ms
201	OFF	<250 ms
401	OFF	<400 ms
101	MIN	<350 ms
201	MIN	<550 ms
401	MIN	<1 s
101	MAX	<3 s
201	MAX	<6 s
401	MAX	<10 s

Network Analyzer

Display: 178 mm (7 in.) diagonal
Scale Resolution: 0.1 dB to 10 dB per division in 0.1 dB steps, independent control for each channel.
Offset Range: +99.9 dB to -99.9 dB in 0.1 dB increments, independent control for each channel.
Display Resolution:
Vertical: 0.003 dB maximum
Horizontal: 101, 201, or 401 points, control panel selectable.
Dynamic Range: +16 dBm to -55 dBm, both channels. Usable to -60 dBm.
Smoothing: Off, Minimum, or Maximum; control panel selectable. Minimum and maximum smoothing use digital and analog techniques to reduce noise on low level traces.
Normalization: During normalization sequence, 800 points for each trace are stored with 0.002 dB resolution for the

Table 1-1. Specifications (Continued)

Network Analyzer (Continued)

full band of the unit. Normalization data are automatically interpolated for ranges less than the full range.

Graticule: Ten vertical divisions. In normal sweep, horizontal divisions are set automatically in frequency increments of a 1, 2, 5 sequence from 1 to 500 MHz. In either of the two alternating sweep modes, there are ten horizontal divisions. Graticule ON/OFF control turns all graticule lines off. Tick marks remain on axis to indicate graticule position.

Markers: Up to eight individually controlled markers, with 10 kHz resolution, can be placed on the display. Amplitude of both traces at active marker is displayed in dB or dBm.

General

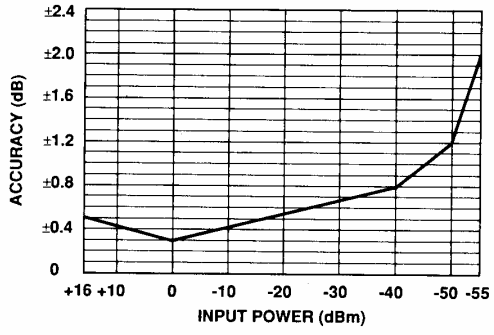
Dimensions: H177 x W430 x D495 mm (7H x 17W x 18-3/4D in.)
Weight: 16 kg (35 lb)
Power: 100, 120, 220, or 240 Vac +6%,-10%; 48-62 Hz; 130 VA maximum
Operating Temperature: 0°C to 50°C

System Accuracy

Transmission Loss Accuracy: Uncertainties resulting from the frequency response of the measurement components are automatically subtracted from test data during the normalization procedure. Overall accuracy is then: Transmission Accuracy = Channel Accuracy + Mismatch Uncertainty.

For channel accuracy, see graph below.

Channel Accuracy:



System Accuracy (Continued)

Typical mismatch uncertainty using 6400 series detectors is ±0.1 dB for a test device with 20 dB return loss and ±0.3 dB for one with 15 dB return loss.

Return Loss Accuracy: Uncertainties resulting from the frequency response of the measurement components are automatically subtracted from test data during the normalization procedure. Overall accuracy is then:
Return Loss Accuracy = Channel Accuracy + SWR Autotester Accuracy

For channel accuracy, see graph below.

6400 series SWR Autotester accuracy is $\pm(0.01 + 0.06\rho^2)$ where ρ is the reflection coefficient of the device under test.

Absolute Power Measurement Accuracy: Absolute Power Measurement Accuracy = Channel Accuracy + Detector Frequency Response

6400 series detector frequency response is ±0.5 dB from 10 to 2000 MHz for the 6409 and ±0.2 dB from 1 to 1000 MHz for the 6407.

Measurement Components

SWR Autotesters: The 6400 series SWR Autotesters are used to make precision return loss measurements. They are available in a variety of connector types and frequency ranges:

Table 1-1. Specifications (Continued)

SWR Autotester Model	Freq. Range (MHz)	Test Port Conn.	Z (Ohms)
6400-6N75	1-1000	N-Male	75
6400-6N75-1	1-2000	N-Male	75
6400-6NF75	1-1000	N-Female	75
6400-6NF75-1	1-2000	N-Female	75
6400-6B50	1-1000	BNC Male	50
6400-6B75	1-1000	BNC Male	75
6400-6N50	1-2000	N Male	50
6400-6NF50	1-2000	N Female	50

Directivity: 40 dB
Maximum Input Power: 27 dBm (500 mW)
Test Port Impedance Match: 1.13 SWR
Insertion Loss (input to test port): 6.5 dB nominal

Detectors: The 6400 series detectors are used to make precision transmission loss or gain and absolute power measurements.

RF Detector Model	Freq. Range (MHz)	Input Conn.	Z (Ohms)
6400-71B50	1-1000	BNC Male	50
6400-71B75	1-1000	BNC Male	75
6400-71N50	1-2000	N Male	50
6400-71N75	1-1000	N Male	75

Maximum Input Power: 20 dBm (100 mW)

SECTION II
INSTALLATION

SECTION II
INSTALLATION

2-1 INTRODUCTION

This section provides information on initial inspection, preparation for use, and General Purpose Interface Bus (GPIB) interconnections. It also includes reshipment and storage information.

2-2 INITIAL INSPECTION

Inspect the shipping container for damage. If the container or cushioning material is damaged, retain until the contents of the shipment have been checked against the packing list and the instrument has been checked for mechanical and electrical operation.

If the analyzer is damaged mechanically, notify your local sales representative or WILTRON Customer Service. If either the shipping container is damaged or the cushioning material shows signs of stress, notify the carrier as well as WILTRON. Keep the shipping materials for the carrier's inspection.

2-3 PREPARATION FOR USE

Preparation for use consists of checking that the line voltage module on the rear panel is set for the correct line voltage. This module can be configured for any of four international, nominal line voltages: 100, 120, 220, or 240 Vac. Before leaving the factory, each analyzer is preset, and fused for the line voltage present in the customer's area. If the actual line voltage is different from that shown on the module, the module can be changed to a different voltage using the procedure in Figure 2-1.

2-4 GPIB SETUP AND INTERCONNECTION

The analyzer provides automated microwave measurements via the GPIB. The following paragraphs provide information about interface connections, cable requirements, and the addressing of the RF analyzer.

2-4.1 Interface Connector

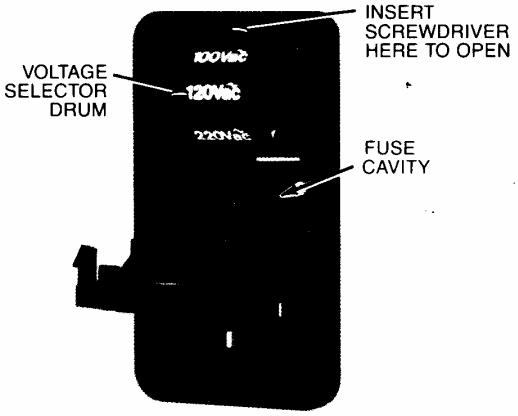
Interface between the analyzer and other devices on the GPIB is via a 24-wire interface cable. This cable uses connector shells having two connector faces. These double-faced connectors allow for the parallel connection of two or more cables to a single device. Figure 2-2 shows the pin assignments for the Type 57 GPIB connector installed on the rear panel.

2-4.2 Cable Length Restrictions

The GPIB system can accommodate up to 15 instruments at any one time. To achieve design performance on the bus, proper timing and voltage level relationships must be maintained. If either the cable length between separate instruments or the accumulated cable length between all instruments is too long, the data and control lines cannot be driven properly and the system may fail to perform. Cable length restrictions are as follows:

1. No more than 15 instruments may be installed on the bus.

2. Total accumulative cable length in meters may not exceed two times the number of bus instruments or 20 meters--whichever is less.



To change the line voltage from that shown on the Line Voltage Selector Module, proceed as follows:

a. Remove the power cord from the line voltage module.

b. Insert the blade of a small screwdriver into the slot at the top-center of the module, and pry open the cover.

c. Remove the voltage selector drum by pulling straight out.

d. Rotate the drum so that the desired line voltage marking faces out, then reinstall the drum.

e. Remove the fuse cartridge from the right-hand fuseholder. The fuse cartridge is identified with a white arrow and is located beneath the voltage selector drum.

f. Check that the proper fuse is installed (see table, below).

g. Change to the correct fuse, if necessary, and replace the fuse cartridge.

h. Close the cover, and ensure that the desired line voltage value is displayed through the opening in the cover.

i. Reinstall the line cord.

Fuse Sizes, Ratings, and Part Numbers

Line Voltage	Area	Fuse Rating	Fuse Size	Wiltron P/N-Fuse	Wiltron P/N-Fuse Holder
100 Vac	Japan	2A, antisurge	3 AG	631-52	533-221
120 Vac	USA	2A, antisurge	3 AG		
220 Vac	Europe	1A, antisurge	5 x 20 mm	631-49	553-240
240 Vac	UK	1A, antisurge	5 x 20 mm		

Figure 2-1. Changing the Line Voltage

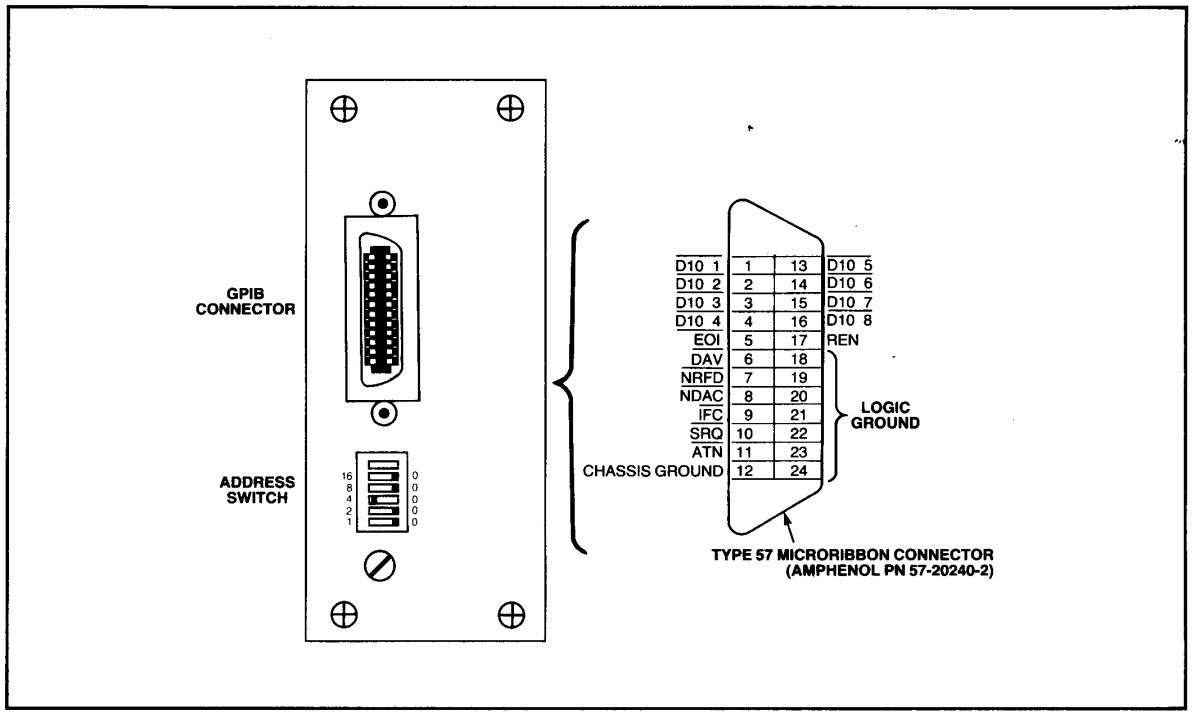


Figure 2-2. GPIB Connector Panel

2-4.3 GPIB Interconnection

The only interconnection required for GPIB operation is between the analyzer and the controller. This interconnection is via a special GPIB cable. The WILTRON Part number for such a cable is 2100-5, -1, -2, or -4 (0.5, 1, 2, or 4 meters in length).

2-4.4 GPIB Address

The analyzer leaves the factory preset to address 5. If a different address is desired, the ADDRESS switches on the GPIB connector panel (Figure 2-2) provide for selecting any address number between 0 and 31. Figure 2-3 shows how to select an address number.

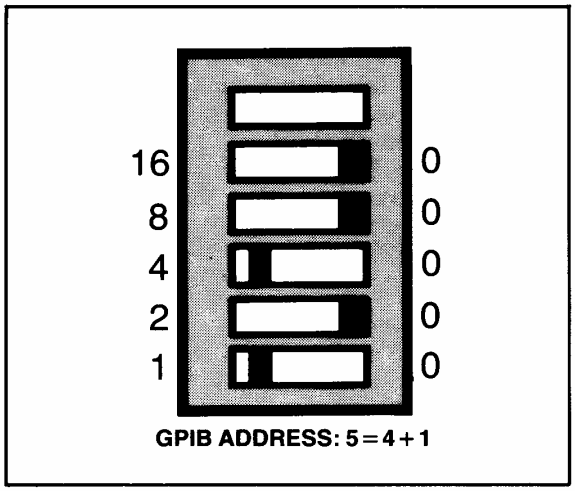


Figure 2-3. Address Selection

2-4.5 Data Delimiting

Data is delimited on the GPIB by either the carriage return (CR) ASCII character or both the carriage return and line feed (CR/LF) ASCII characters. The 6400 software accomodates either character automatically.

2-5 PREPARATION FOR STORAGE AND/OR SHIPMENT

Paragraphs 2-5.1 and 2-5.2 give instructions for preparing the analyzer for storage or shipment.

2-5.1 Preparation for Storage

Preparing the analyzer for storage consists of cleaning the unit, packing the inside with moisture-absorbing dessicant crystals, and storing the unit in a temperature environment that is maintained between -40 and +70 degrees centigrade.

2-5.2 Preparation for Shipment

To provide maximum protection against damage in transit, the analyzer should be repackaged in the original shipping container. If this container is no longer available and the analyzer is being returned to WILTRON for repair, advise WILTRON Customer Service; they will send a new shipping container free of charge. In the event neither of these two options is possible, instructions for packaging and shipment are given below.

a. Use a Suitable Container. Obtain a corrugated cardboard carton with a 275-pound test strength. This carton should have inside dimensions of no less than six inches larger than the instrument dimensions to allow for cushioning.

b. Protect the Instrument. Surround the instrument with polyethylene sheeting to protect the finish.

c. Cushion the Instrument. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument. Provide at least three inches of dunnage on all sides.

d. Seal the Container. Seal the carton by using either shipping tape or an industrial stapler.

e. Address the Container. If the instrument is being returned to WILTRON for service, mark the WILTRON address and your return address on the carton in one or more prominent locations. For international customers, use the address of your local representative (see Table 2-1). For U.S.A. customers, use the WILTRON address shown below:

WILTRON Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Table 2-1. WILTRON Company International Sales Representatives

ARGENTINA
I.A. ELECTRONICA S.R.L.
T.C. de Allende 430
5000 Cordoba
Telephone: (051) 32150/34815
Telex: 390 51894 ENTOP AR

AUSTRALIA
KENELEC (AUST.) PTY. LTD.
48 Henderson Road
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Xi Jiao, Er-Li Kou Beijing
Telephone: 890931
Telex: 716-22304 CMIEC CN

CHINA ELECTRONICS IMPORT & EXPORT CORPORATION
49 Fuxing Road, Beijing
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Telex: 303-2645 ELEPEX

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Telex: 855-37163

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ALKAN ESTABLISHMENT
2 El Mesaha Square, Dokki, A.R.E.
P.O. Box 1913, Cairo 11511
Telephone: (2) 987114
Telex: 927-93644 ALKAN UN & 92096 EKA UN

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INSTRUMENTARIUM ELEKTRONIIKKA
P.O. Box 64, Vitikka 1
SF-02631 ESPOO
Telephone: 358 (0) 5281
Telex: 857-124426 HAVUL or 857-8100155 INSTRUE
Teletex: 100155
Fax: (0) 524986

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Field Service Centre
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Telex: 0314890

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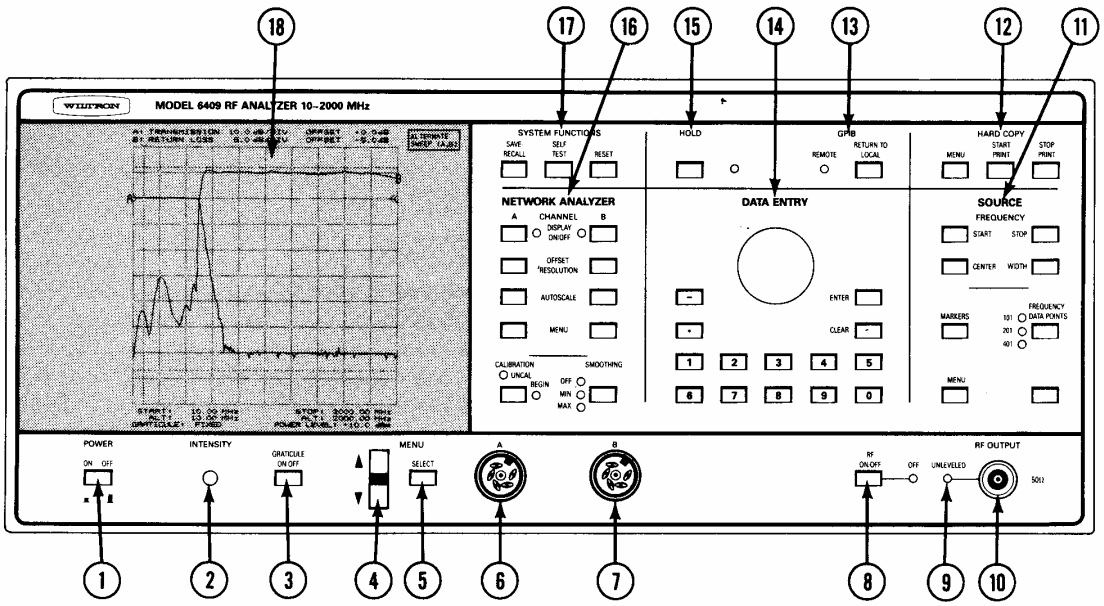
SECTION III
LOCAL (FRONT PANEL) OPERATION



(1) **POWER ON/OFF:** Turns the instrument on and off. When pressed to ON, it initiates an instrument self test.

(2) **INTENSITY:** Adjusts the intensity of the display.

(3) **GRATICULE ON/OFF:** Turns the display graticule on and off. Tick marks showing where the graticule lines would be are displayed when the graticule is off.

(4) **MENU UP/DOWN Switch:** Moves menu cursor up or down to select between menu options.

(5) **SELECT:** Implements the selected menu option, when its use is indicated by instructions on the CRT.

(6) **A Connector:** Provides input for Channel A.

(7) **B Connector:** Provides input for Channel B.

(8) **RF ON/OFF:** Turns the RF energy on and off. Indicator is lit when the RF is off.

(9) **UNLEVELED:** Lights when the output is unleveled.

(10) **RF OUTPUT Connector:** Provides a 50-ohm output port for RF energy. Optional 75-ohm output is available for 6407.

(11) **SOURCE Keys and Indicators:** Control RF source functions. Refer to paragraph 3-2.6 for detailed key descriptions.

(12) **HARD COPY Keys:** Initiates a hard-copy printout of measurement results. Refer to paragraph 3-2.5 for detailed key descriptions.

(13) **GPIB Indicator and Key:** Key returns the analyzer to local (control panel) operation. Indicator is lit when the analyzer is in the GPIB mode. Refer to paragraph 3-2.7 for detailed indicator and key descriptions.

(14) **DATA ENTRY Keys and Knob:** Enter numerical data. Refer to paragraph 3-2.4 for detailed key descriptions.

(15) **HOLD:** Freezes the data, which can then be manipulated (1) by adding or changing limit or marker values or (2) by changing offset or resolution values. Indicator is lit while the data are frozen, which occurs when the HOLD or START PRINT keys are activated.

(16) **NETWORK ANALYZER Keys and Indicators:** Control network analyzer and displayed trace functions. Refer to paragraph 3-2.3 for detailed key and indicator descriptions.

(17) **SYSTEM FUNCTIONS Keys:** Saves and recalls front panel setups, self tests the analyzer, and resets the front panel to factory selected settings. Refer to paragraph 3-2.2 for detailed key descriptions.

(18) **CRT:** Displays Channel A and B traces, network analyzer and RF source parameters, and control and calibration menus. Refer to paragraph 3-2.1 for a detailed description.

Figure 3-1. Model 6409 RF Analyzer Front Panel Controls

SECTION III
LOCAL (CONTROL PANEL) OPERATION

3-1 INTRODUCTION

This section describes the operation of the Models 6407 and 6409 RF Analyzer using the control panel controls. It describes the controls and rear panel connectors; how to make transmission, return loss, power, and alternating sweep measurements; and how to check that the instrument is operating properly.

3-2 CONTROL PANEL CONTROLS

Operation of the control panel controls is described in Figure 3-1 and in paragraphs 3-2.1 thru 3-2.7.

3-2.1 CRT Display (Figure 3-2)

The CRT displays the measurement traces and the present settings for the NETWORK ANALYZER and frequency SOURCE controls:

a. CRT Screen: Displays (1) either the respective outputs of channels A and B on traces A and B, (2) the Channel A signal alternating between traces A and B or (3) the Channel A signal on trace A alternating with the Channel B signal on trace B. See Figure 3-19 on page 3-11 for a description of the alternating sweep mode.

b. NETWORK ANALYZER Settings: The two lines labeled "A" and "B" across the top of the screen display the type of measurement selected and the offset and vertical resolution values set for traces A and/or B.

c. SOURCE Mode Selection: The source mode is displayed in the box in the top-right side of the screen. This box displays "SWEEP" when a normal sweep has been selected, "ALTERNATE SWEEP (A)" (or A,B)" when an alternat-

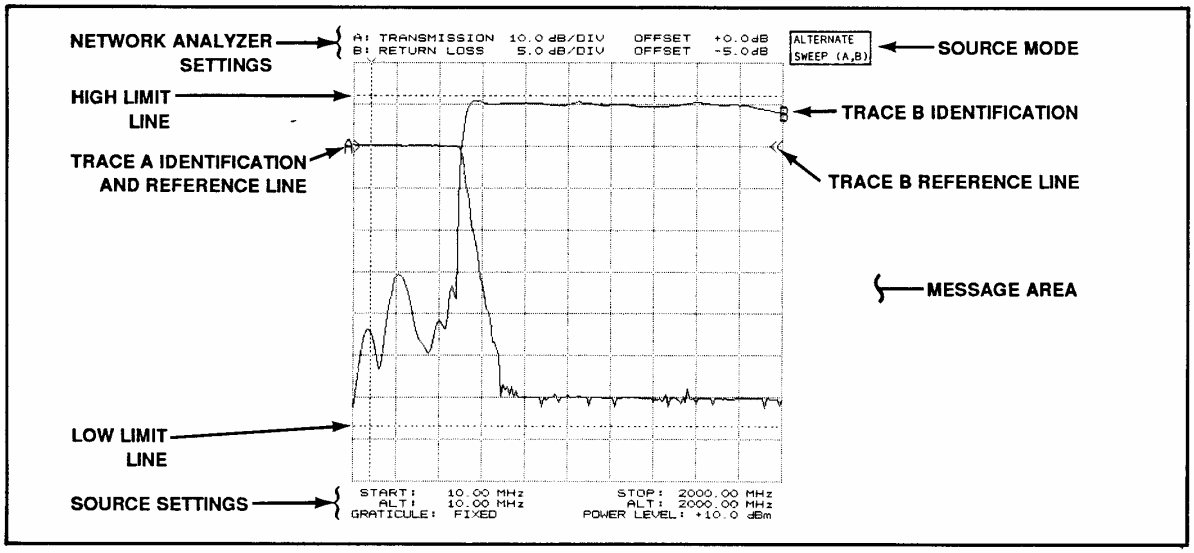


Figure 3-2. CRT Display

ing sweep has been selected, "RF OFF" when the RF output has been turned off, or "HOLD" when the instrument is in the HOLD mode.

d. SOURCE Frequency and Power and Horizontal Resolution (GRATICULE) Settings: The three lines along the bottom of the screen display the
   (1) source start/stop frequencies,
   (2) alternate sweep start/stop frequencies,
   (3) RF power setting and horizontal resolution (GRATICULE) of the displayed traces.

   In the normal-sweep mode, the horizontal resolution and intelligent-graticule divisions are automatically chosen for optimum display of the selected frequency-sweep width.

   In either of the two alternate-sweep modes, the graticule is fixed at 10 vertical and 10 horizontal divisions.

3-2.2 SYSTEM FUNCTIONS Keys (Figure 3-3)

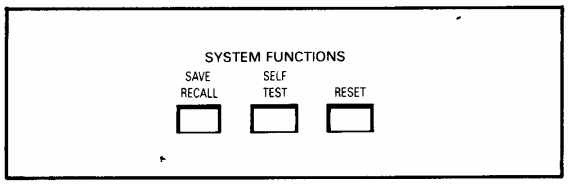


Figure 3-3. SYSTEM FUNCTIONS Keys

The SYSTEM FUNCTIONS keys are described below.

a. SAVE/RECALL Key: Displays a menu (Figure 3-4) that lets the operator SAVE the current control panel setting or RECALL any of nine stored front panel setups. The MENU rocker switch (Figure 3-1) is used to make the selection. Should this key be pressed and then not wanted, the DATA ENTRY CLEAR (Figure 3-10) key can be used to cancel the key action.

b. SELF TEST Key: Initiates a self test of the analyzer. If the analyzer functions properly, the screen displays "ALL TESTS PASSED." If the self test re-

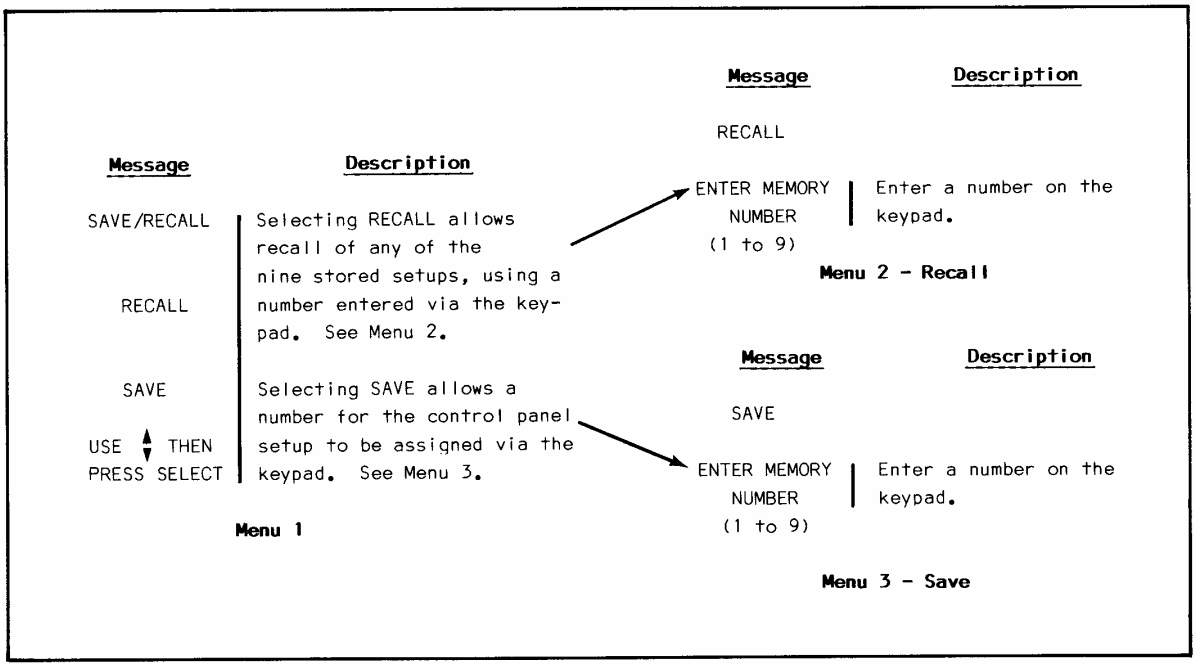


Figure 3-4. SAVE/RECALL Key Menus

veals a problem, the screen displays a failure message instead. Also at the end of the self test the screen displays the GPIB address, if Option 3 is fitted.

c. RESET Key: Displays a menu (Figure 3-5) that lets the operator use the MENU SELECT key (Figure 3-1) to restore the factory-selected control panel settings. The settings for the 6409 and 6407 (in parenthesis) are shown below.

```
Channel A: TRANSMISSION
Channel A: OFFSET: 0.0 dB
Channel A: RESOLUTION: 10 dB/Division
Channel B: RETURN LOSS
Channel B: OFFSET: 0.0 dB
Channel B: RESOLUTION: 10 dB/Division
Source Mode: Normal SWEEP
START Frequency: 10 MHz (1 MHz)
STOP Frequency: 2000 MHz (1000 MHz)
POWER LEVEL: 10 dBm
SMOOTHING: OFF
FREQUENCY DATA POINTS: 201
```

3-2.3 NETWORK ANALYZER Keys and Indicator (Figure 3-6)

The NETWORK ANALYZER keys and indicator described below are the same for both channels A and B. Generally, should one of these keys be pressed and then not wanted, the DATA ENTRY CLEAR (Figure 3-10) key can be used to cancel the key action.

Message	Description
RESET	
PRESS SELECT TO RESTORE DEFAULTS	Press the MENU SELECT key to restore the factory selected control panel settings.
PRESS CLEAR TO RETURN TO MEASUREMENT MODE	Press the DATA ENTRY CLEAR key to return to the measurement mode
CALIBRATION DATA IS NOT AFFECTED	Calibration data is not affected by the RESET key.

Figure 3-5. RESET Key Menu

a. DISPLAY ON/OFF Key and Indicator: Key turns its associated trace and

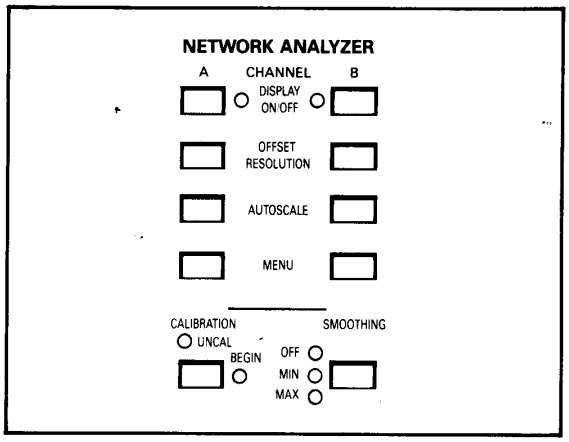


Figure 3-6. NETWORK ANALYZER Keys and Indicator

limits/reference line on or off. The associated indicator is lit when the trace is on.

b. MENU Key: Displays a menu (Figure 3-7) that lets the operator select the measurement type, set test limits, or move the reference line.

c. AUTOSCALE Key: Sets the associated trace at optimum offset and resolution values for viewing the measured data.

d. OFFSET/RESOLUTION Key: Displays a menu (Figure 3-8) that lets the operator select OFFSET or RESOLUTION.

e. CALIBRATION Key: Displays a series of instructions (Figure 3-9) that guide the operator through a calibration cycle.

f. UNCAL Indicator: Lights when either measurement trace is uncalibrated.

g. BEGIN Indicator: Lights at the beginning of a calibration cycle and remains lit until the cycle is completed.

h. SMOOTHING Key and Indicators: Key provides two levels of filtering, MIN and MAX, that improve the display at low-signal levels. OFF indicator is lit when no smoothing (low-level filtering) is supplied.

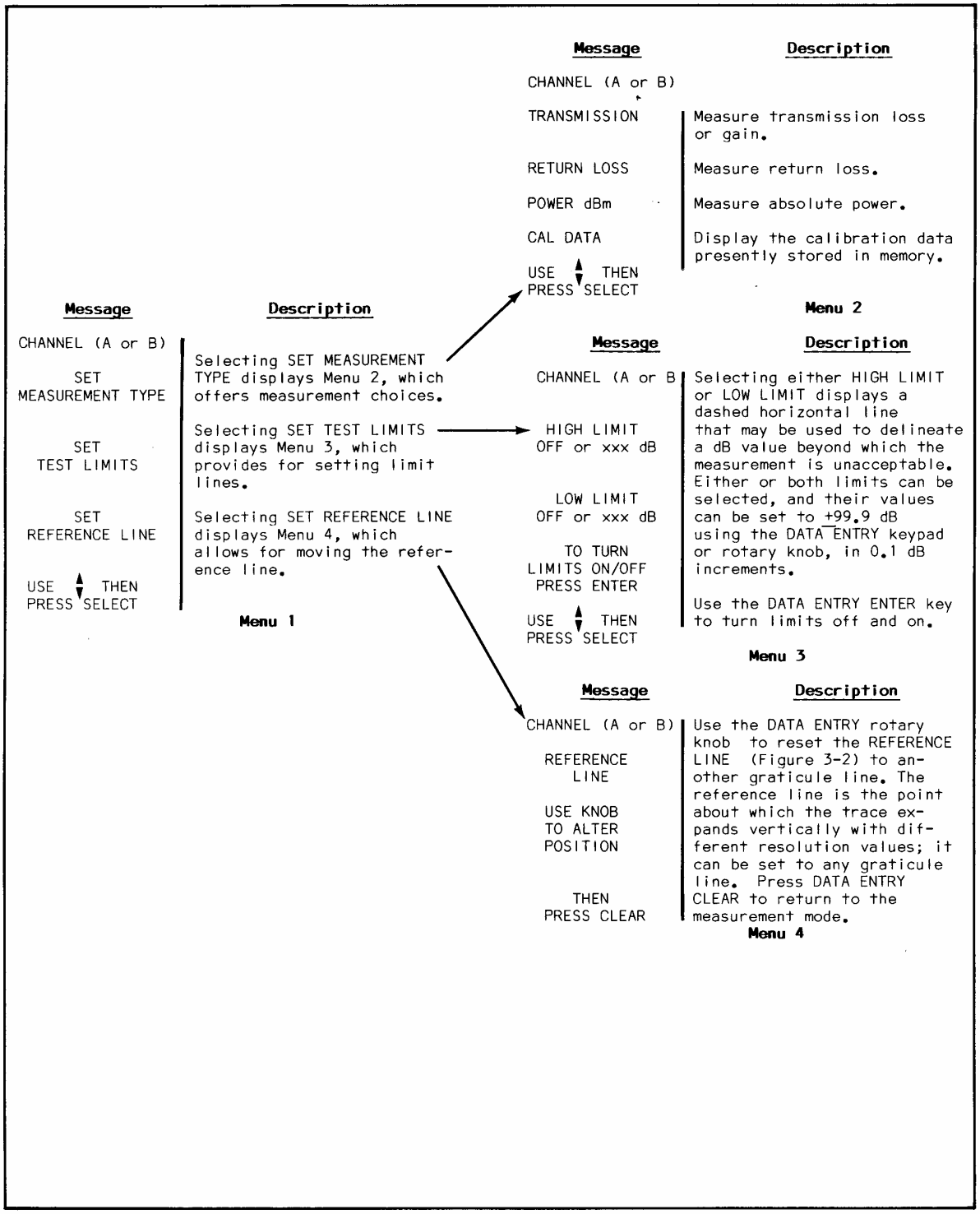


Figure 3-7. Channel A/B MENU Menus

Message	Description
CHANNEL (A or B)	Selecting OFFSET provides for using the keypad or rotary knob to set the value of the reference line (Figure 3-2). Values from 0.0 dB to ±99.9 dB, in increments of 0.1 dB, are possible.
OFFSET nnnn dB RESOLUTION nnnn dB/Div	Selecting RESOLUTION provides for using the keypad or rotary knob to set the display vertical resolution. Values from 0.1 to 10 dB, in increments of 0.1 dB, are possible when using the keypad. The rotary knob allows adjustments in 1, 2, and 5 dB values.
USE ▲▼	Use MENU rocker switch to make selection.

Figure 3-8. OFFSET/RESOLUTION Key Menu

Calibration is the process whereby losses inherent in a transmission or return loss measurement system are measured, stored in internal memory, and later subtracted so that the results displayed are those of the test device, minus residual losses. Pressing the CALIBRATION key initiates the following sequence of menus when the Channel A trace has been selected to display transmission loss or gain and the Channel B trace return loss. Important: Set output power for the desired level before beginning the calibration sequence.

Message	Description
CALIBRATION MODE	Places the network analyzer section in the calibration mode.
PRESS SELECT TO BEGIN CALIBRATION	Press the MENU SELECT key (Figure 3-1) to display the first calibration menu.
PRESS CLEAR TO RETURN TO MEASUREMENT MODE	Press the DATA ENTRY CLEAR key to return to the network analyzer section to the measurement mode last exited. At this point, the calibration data has not been affected.
TRANSMISSION CALIBRATION	Connect the RF Input port on the SWR Autotester to the RF OUTPUT port on the sweep generator.
CONNECT CHANNEL A DETECTOR TO TEST PORT	Connect the RF detector between connector A and the Test Port on the SWR Autotester. NOTE When only transmission loss is being measured and the SWR Autotester is not being used, the test port called out in the menu is the port to which the test device connects. In most cases, it will be the RF OUTPUT port on the analyzer.
PRESS SELECT WHEN READY	Press the MENU SELECT key to store the residual losses inherent in both the detector and the connection.

Figure 3-9. CALIBRATION Key Menus (Page 1 of 2)

Message	Description
RETURN LOSS CALIBRATION STEP 1	
CONNECT SWR AUTOTESTER TO CHANNEL A AND CONNECT OPEN TO TEST PORT	Connect the SWR Autotester to connector A. Connect the end of the Model 22N Open/Short labeled "OPEN" to the Test Port on the SWR Autotester.
PRESS SELECT WHEN READY	Press the MENU SELECT key to store the measurement results.
RETURN LOSS CALIBRATION STEP 2	
REMOVE OPEN AND CONNECT SHORT TO TEST PORT	Reverse ends on the Model 22N Open/Short. Press the MENU SELECT key to store an average value of the open and short measurements. Internal software has averaged the losses measured when the open was installed with those measured when the short was installed.
PRESS SELECT WHEN READY	
CALIBRATION COMPLETED	The calibration cycle is now complete. The losses inherent in the SWR Autotester, Type N-to-N Adapter, and RF detector have been measured and stored. In all future measurements of test devices at this level of output power, these losses will be subtracted from measured losses; consequently, the results displayed will be those of the test device minus residuals.
CONNECT TEST DEVICE	
PRESS SELECT WHEN READY	

Figure 3-9. CALIBRATION Key Menus (Page 2 of 2)

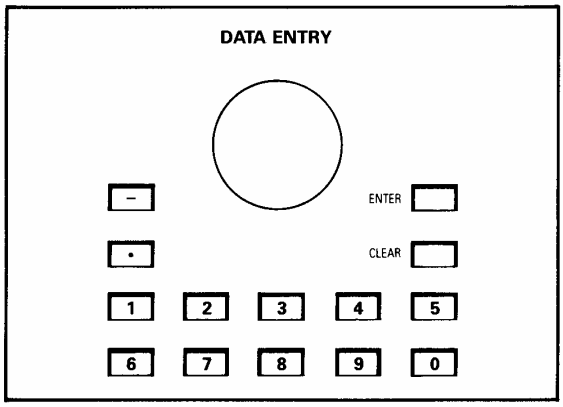


Figure 3-10. DATA ENTRY Keys and Knob

3-2.4 DATA ENTRY Keys and Knob (Figure 3-10)

The DATA ENTRY keys and knob are described below.

a. Knob: Alters measurement values.

b. Keypad: Enters measurement values.

c. ENTER Key: Terminates data entries made from the keypad and provides on/off control for limits (paragraph 3-2.3b) and markers (paragraph 3-2.6e).

d. CLEAR Key: Clears an entered value, if pressed before the ENTRY key. This key can also be used to clear a displayed menu.

3-2.5 HARD COPY Keys (Figure 3-11)

The HARD COPY keys are described below.

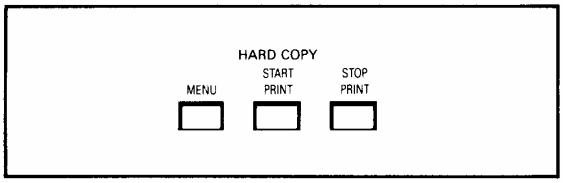


Figure 3-11. HARD COPY Keys

a. MENU Key: Displays a menu (Figure 3-12) that lets the operator select between printing either the graphic display or a tabulation of the measured values.

b. START PRINT Key: Freezes the displayed data and starts printing it. The type of printout then obtained, graphic or tabulated, is based on the last MENU key menu selection.

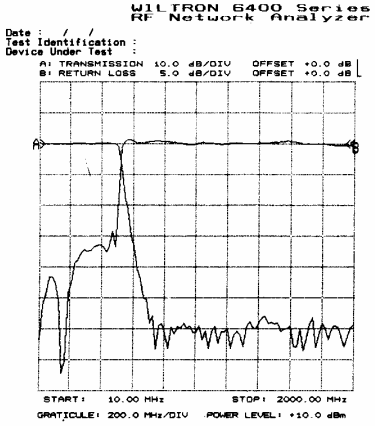
c. STOP PRINT Key: Stops printing the data immediately.

Message	Description
HARD COPY MENU	
PRINT GRAPH	Selecting PRINT GRAPH prints the on-screen graphic when the MENU SELECT key is pressed.
TABULAR: 26 POINTS 51 POINTS 101 POINTS 201 POINTS 401 POINTS	Selecting one of the tabular options prints out a data tabulation at either 26, 51, 101, 201 or 401 frequency points.
MARKERS ONLY	Selecting MARKERS ONLY prints data only at the marker frequencies. Figure 3-13 shows samples of hard-copy printouts.
USE ▲ ▼ THEN PRESS SELECT	Pressing SELECT starts the printing.

Figure 3-12. HARD COPY Menu

3-2.6 SOURCE Keys and Indicators (Figure 3-14)

The SOURCE keys and indicators are described below. Should one of these keys be pressed and then not wanted, the DATA ENTRY CLEAR (Figure 3-10) key can be used to cancel the key action.



WILTRON 6400 Series
RF Network Analyzer

Date : / /
Test Identification :
Device Under Test :

A: TRANSMISSION 10.0 dB/DIV OFFSET +0.0 dB
B: RETURN LOSS 5.0 dB/DIV OFFSET +0.0 dB

START: 10.00 MHz STOP: 2000.00 MHz
GRATICULE: 200.0 MHz/DIV POWER LEVEL: +10.0 dBm

---------- Additional Instrument Information ----------

Channel A: High Limit : --- off --- Low Limit : --- off ---
Channel B: High Limit : --- off --- Low Limit : --- off ---

Freq Data Points : 101 Smoothing : OFF Power Level : +10.00 dBm

---------- Markers ---------- ----- Readout --- off ---

M1 : --- off --- M5 : --- off ---
M2 : --- off --- M6 : --- off --- Amplitude A : --- off ---
M3 : --- off --- M7 : --- off ---
M4 : --- off --- M8 : --- off --- Amplitude B : --- off ---

"PRINT GRAPH" Option Printout

WILTRON 6400 Series
RF Network Analyzer

Date : / /
Test Identification :
Device Under Test :

	FREQUENCY	A:TRANSMISSION	B:RETURN LOSS	
	10.00 MHz	-0.04 dB	-31.85 dB	
	29.90 MHz	-0.04 dB	-26.21 dB	
	49.80 MHz	-0.04 dB	-24.40 dB	
	69.70 MHz	-0.05 dB	-21.76 dB	
(1)	**100.11 MHz**	**-0.04 dB**	**-21.72 dB**	.MARKER
	189.50 MHz	-0.07 dB	-33.77 dB	
	129.40 MHz	-0.11 dB	-25.71 dB	
	149.30 MHz	-0.12 dB	-37.15 dB	
	169.20 MHz	-0.09 dB	-35.30 dB	
(2)	**200.00 MHz**	**-0.04 dB**	**-24.22 dB**	.MARKER
	209.00 MHz	-0.01 dB	-22.45 dB	
	228.90 MHz	+0.07 dB	-19.37 dB	
	248.80 MHz	+0.17 dB	-18.84 dB	
	268.70 MHz	+0.10 dB	-17.81 dB	
(3)	**300.00 MHz**	**+0.02 dB**	**-17.48 dB**	.MARKER
	308.50 MHz	-0.02 dB	-17.55 dB	
	328.40 MHz	-0.01 dB	-17.34 dB	
	348.30 MHz	-0.01 dB	-16.89 dB	
	368.20 MHz	+0.00 dB	-16.57 dB	
(4)	**400.00 MHz**	**+0.05 dB**	**-16.53 dB**	.MARKER
	408.00 MHz	+0.09 dB	-16.77 dB	
	427.90 MHz	+0.10 dB	-17.58 dB	
	447.80 MHz	+0.00 dB	-16.56 dB	
	467.70 MHz	-0.17 dB	-14.37 dB	
(5)	**500.00 MHz**	**-0.15 dB**	**-16.77 dB**	.MARKER
	507.50 MHz	-1.52 dB	-10.70 dB	
	527.40 MHz	-8.18 dB	-0.57 dB	
	547.30 MHz	-17.57 dB	+0.40 dB	
	567.20 MHz	-21.88 dB	+0.54 dB	
(6)	**600.00 MHz**	**-30.43 dB**	**+0.54 dB**	.MARKER
	607.00 MHz	-33.98 dB	+0.33 dB	
	626.90 MHz	-41.22 dB	+0.08 dB	
	646.80 MHz	-44.52 dB	+0.09 dB	
	666.70 MHz	-50.50 dB	+0.00 dB	
(7)	**700.00 MHz**	**-51.43 dB**	**+0.17 dB**	.MARKER
	706.50 MHz	-57.86 dB	+0.26 dB	
	726.40 MHz	-66.74 dB	+0.35 dB	
	746.30 MHz	-59.77 dB	+0.43 dB	
	766.20 MHz	-64.01 dB	+0.36 dB	
(8)	**800.00 MHz**	**-61.30 dB**	**+0.29 dB**	.READOUT
	805.00 MHz	-66.71 dB	+0.31 dB	
	825.90 MHz	-66.06 dB	+0.29 dB	
	845.80 MHz	-60.95 dB	+0.26 dB	
	865.70 MHz	-64.66 dB	+0.14 dB	
	885.60 MHz	-66.64 dB	+0.11 dB	
	905.50 MHz	-61.48 dB	+0.05 dB	
	925.40 MHz	-66.61 dB	-0.09 dB	
	945.30 MHz	-66.60 dB	-0.18 dB	
	965.20 MHz	-61.77 dB	-0.17 dB	
	985.10 MHz	-65.07 dB	-0.15 dB	

Page : 1

"TABULAR" Option Printout

WILTRON 6400 Series
RF Network Analyzer

Date : / /
Test Identification :
Device Under Test :

	FREQUENCY	A:TRANSMISSION	B:RETURN LOSS	
(1)	**100.11 MHz**	**-0.04 dB**	**-21.72 dB**	.MARKER
(2)	**200.00 MHz**	**-0.04 dB**	**-24.19 dB**	.MARKER
(3)	**300.00 MHz**	**+0.07 dB**	**-17.41 dB**	.MARKER
(4)	**400.00 MHz**	**+0.05 dB**	**-16.53 dB**	.MARKER
(5)	**500.00 MHz**	**-0.15 dB**	**-16.81 dB**	.MARKER
(6)	**600.00 MHz**	**-30.45 dB**	**+0.54 dB**	.MARKER
(7)	**700.00 MHz**	**-52.74 dB**	**+0.16 dB**	.MARKER
(8)	**800.00 MHz**	**-60.26 dB**	**+0.28 dB**	.READOUT
	2000.00 MHz	-66.10 dB	-0.32 dB	

"MARKERS ONLY" Option Printout

Figure 3-13. Hard-Copy Printouts (Samples)

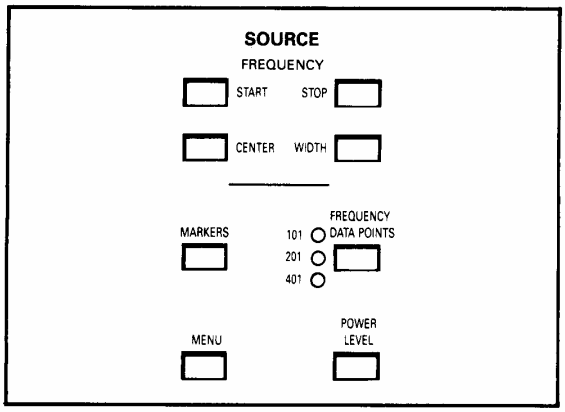


Figure 3-14. SOURCE Keys and Indicators

a. FREQUENCY START Key: Displays a menu that allows frequency entry (Figure 3-15).

b. FREQUENCY STOP Key: Displays a menu that allows frequency entry (Figure 3-15).

c. FREQUENCY CENTER Key: Displays a menu that allows frequency entry (Figure 3-16).

d. FREQUENCY WIDTH Key: Displays a menu that allows frequency entry (Figure 3-16).

e. MARKERS Key: Displays a menu that allows you to enter the frequency at which the marker displays (Figure 3-17).

f. FREQUENCY DATA POINTS Key and Indicators: Key selects 101, 201, or 401 voltage steps for the digital-sweep ramp. The highest number provides the finest frequency-sweep resolution.

g. MENU Key: Displays a menu (Figure 3-19) that allows for selecting a normal or an alternating sweep mode.

h. POWER LEVEL Key: Opens the output-power parameter and allows the DATA ENTRY keypad or rotary knob to be used to enter a new power level in dBm. Use the ENTER key to terminate the power-level entry.

Message	Description
ENTER START nnnn MHz ENTER STOP nnnn MHz	Enter a new START or STOP frequency. If the menu is a result of pressing the START key, that parameter is open for frequency modification; the STOP parameter can be accessed using the MENU rocker switch. If the menu is a result of pressing the STOP key, the STOP parameter is open and the START parameter can be accessed with the rocker switch. In either case, the frequency can be changed in increments of 0.01 MHz, via the DATA ENTRY keypad or rotary knob. The start frequency must be less than or equal to the stop frequency.

Figure 3-15. FREQUENCY START or STOP Key Menu

Message	Description
ENTER CENTER nnnn MHz ENTER WIDTH nnnn MHz	Enter a CENTER or WIDTH frequency. If the menu is a result of pressing the CENTER key, that parameter is open for frequency modification; the WIDTH parameter can be accessed using the MENU rocker switch. If the menu is a result of pressing the WIDTH key, the WIDTH parameter is open and the CENTER parameter can be accessed with the rocker switch. The frequency is entered via the DATA ENTRY keypad or rotary knob. A warning message displays if the width entry is too wide.

Figure 3-16. FREQUENCY CENTER or WIDTH Key Menu

Message	Description
MARKERS MENU M1: nnnnn M2: nnnnn M3: nnnnn M4: nnnnn M5 TO M8 READOUT (Mx) A: nnnnn dB B: nnnnn dB SELECT FOR ALL MARKERS or SELECT FOR READOUT ONLY PRESS ENTER FOR ON/OFF	1. Select one of the M1-M8 parameters as the active marker, using the MENU rocker switch and SELECT key. The active marker, the one currently highlighted, is open for frequency entry or modification. The power at this point on the A trace, B trace, or both, appears in the READOUT (Mx) area. 2. Enter a frequency from the keypad or change the frequency using the keypad or rotary knob. 3. Select M5 TO M8 to display a listing for markers M5 to M8. Pressing the MENU SELECT key repeatedly toggles all of the displayed markers on and off, except for the active marker. Pressing SELECT also toggles the "ALL MARKERS" or "READOUT ONLY" menu entries. Pressing the DISPLAY ENTRY ENTER key turns the active marker off and on.

All M1-M8 parameters that have been assigned frequencies are displayed on the screen as dashed-vertical lines (Figure 3-18). The active marker, the one currently highlighted, has a caret symbol (V) at its top.

Figure 3-17. SOURCE MARKERS Key Menus

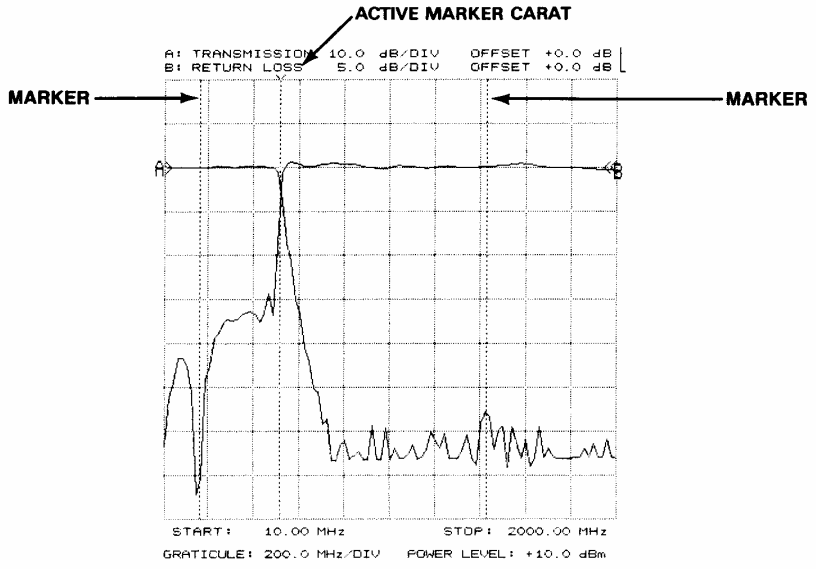


Figure 3-18. Frequency Marker Screen Display

Message	Description
SOURCE MENU	NORMAL is the single, or non-alternating mode. ALTERNATE is the alternating sweep mode.
SET SWEEP TYPE	Selecting NORMAL displays "SWEEP" in the box at the top-right and "START" or "CENTER" and "STOP" or "WIDTH" in the frequency line under the CRT graticle. Use the FREQUENCY START, STOP or CENTER, WIDTH keys to change the displayed values.
NORMAL	Selecting ALTERNATE Input A displays "ALTERNATE SWEEP A" on the CRT and applies the main and alternate sweeps to Input A. The main sweep displays on Trace A, via Channel A, and the alternate sweep on Trace B, via Channel B. The sweep limits of both sweeps are shown on the CRT. Use the FREQUENCY START/STOP or CENTER/WIDTH keys (as appropriate) to change the limits of the alternate sweep.
ALTERNATE Input A	
ALTERNATE Input A, B	Selecting ALTERNATE Input A and B displays "ALTERNATE SWEEP A, B" on the CRT and applies the main and alternate sweeps to both channels. The Channel A output is associated with the main sweep and the Channel B output with the alternate sweep. The main sweep displays on trace A and the alternate sweep on trace B. The sweep limits for both sweeps are shown on the CRT. Use the FREQUENCY START/STOP or CENTER/WIDTH keys (as appropriate) to change the limits of the alternate sweep.
USE ▲▼ THEN PRESS SELECT	

Figure 3-19. SOURCE MENU Key Menu

3-2.7 GPIB Indicator and Key (Figure 3-20)

a. REMOTE Indicator: Lights when in the the remote (GPIB) mode. When lit, a menu providing GPIB status (Figure 3-21) displays in the MENU area of the screen (Figure 3-2).

b. RETURN TO LOCAL Key:
   (1) If pressed while in the GPIB mode, the analyzer returns to the local mode. This occurs unless the local lockout (LLO) message has been programmed, in which case the key causes no action.
   (2) If pressed while in the local mode, the analyzer's GPIB address displays in the MENU area of the screen (Figure 3-22).

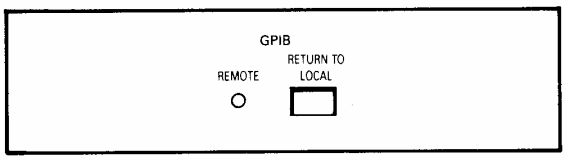


Figure 3-20. GPIB Indicator and Key

```
  GPIB
 STATUS

  TALK: ●
LISTEN: o
   SRQ: o
 LOCAL
LOCKOUT: o
REMOTE: o
```

Associated indicator lights when analyzer is respectively talking, listening, generating an SRQ, or is in the local lockout or remote mode.

Figure 3-21. GPIB Status Display

Message	Description
GPIB ADDRESS nn	"nn" is the listen address number set using the rear panel ADDRESS switch.

Figure 3-22. GPIB Address Display

3-3 REAR PANEL CONNECTORS

The rear panel contains multipin GPIB and printer connectors, the GPIB address

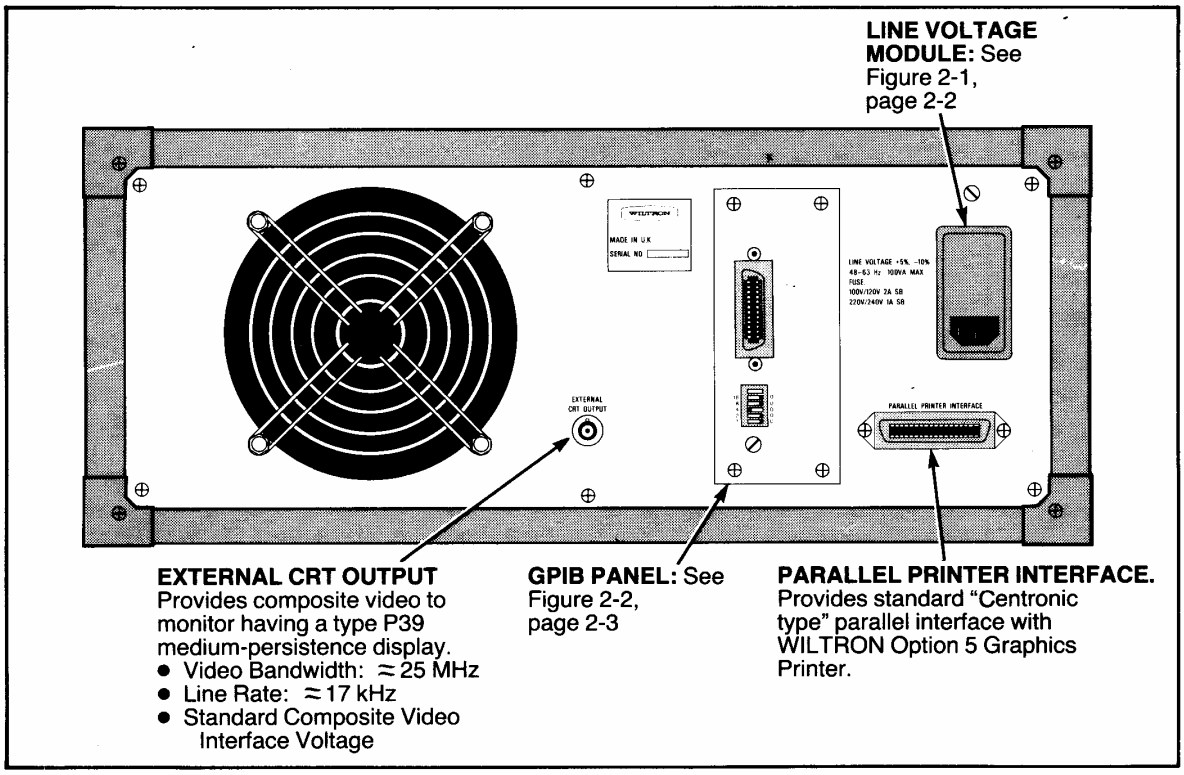


Figure 3-23. Rear Panel Connectors

switches, a composite-video BNC connector, and the line voltage module. The line voltage module and GPIB connector and address switches are described in Section II; the printer and composite-video connectors are described in Figure 3-23.

3-4 MEASUREMENTS WITH THE RF ANALYZER

The 6407 and 6409 RF Analyzers can be used to make transmission loss or gain, return loss, absolute power, or alternating sweep measurements.

3-4.1 Transmission and Return Loss Measurements

How to make a transmission and return loss measurement is described in Table 3-1; a test setup is shown in Figure 3-24.

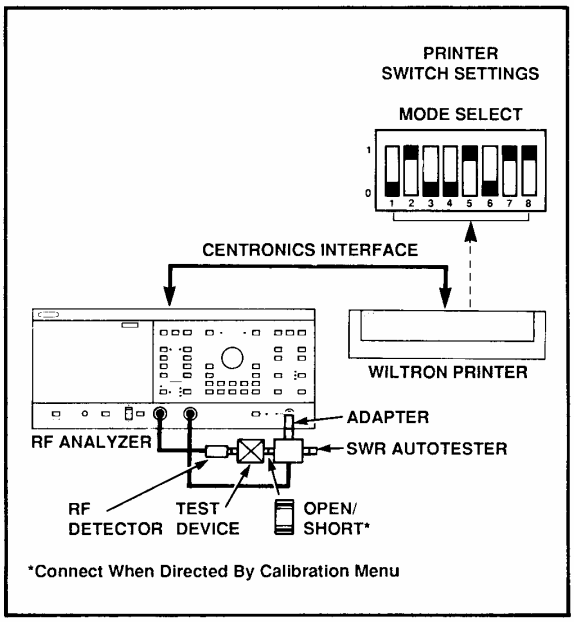
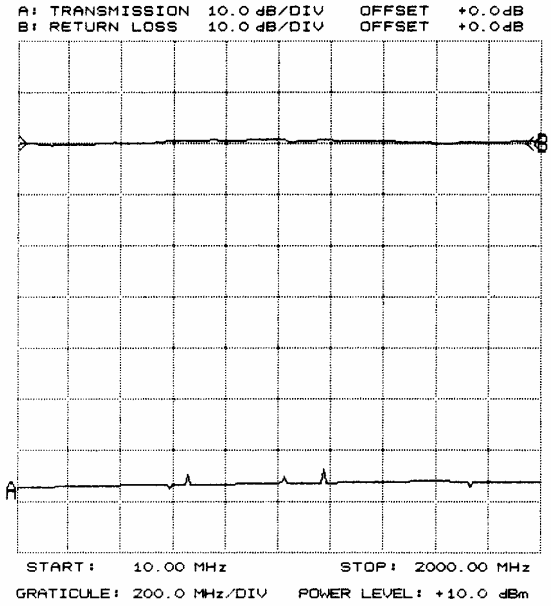


Figure 3-24. Test Setup for Transmission and Return Loss

Table 3-1. Making Transmission and Return Loss Measurements -

1. Connect test equipment per Figure 3-24, except do not connect the test device; turn the printer on.

2. Press POWER on the analyzer to on. At the conclusion of the built-in self test, the screen displays "ALL TESTS PASSED," and the CRT resembles that shown below. Control settings may be different from those shown, which are the RESET control settings (6409). The instrument comes on line with the same control settings it had when last turned off. Ensure that both channels are on and that Channel A is set for TRANSMISSION and Channel B for RETURN LOSS.



Screen Display with Factory Selected Control Settings

3. Press the NETWORK ANALYZER CALIBRATION key and follow the directions given in the calibration-cycle sequence of menus. If necessary, refer to Figure 3-9 for an explanation of the menus. After finishing the calibration, connect the test device and RF detector as shown in Figure 3-24.

Transmission Loss Measurement

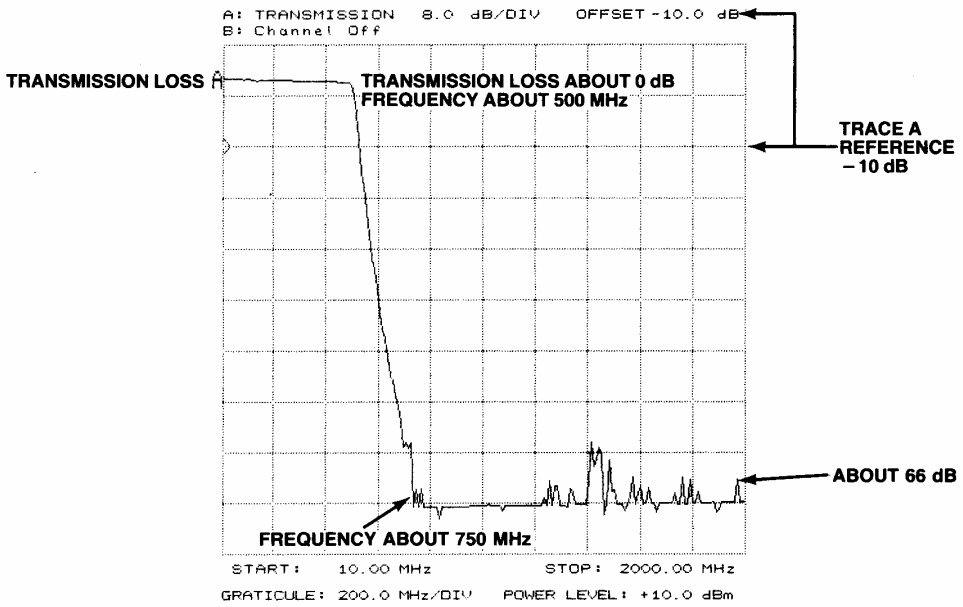
4. Measure the transmission loss, as follows:

   a. Press the Channel B DISPLAY ON/OFF key to off.

Table 3-1. Making Transmission and Return Loss Measurements (Continued)

b. Press the Channel A AUTOSCALE key. This gives an optimum vertical display of the test data.

5. Read the transmission loss by interpolating the displayed graphic as described below, or read it directly using the markers and readout function as described in step 6. In the example shown below, the test device is a 500 MHz low pass filter.



By interpolating the display, we see that the pass band begins to drop at about 500 MHz, and that the skirt bottoms out at about 750 MHz. The transmission loss is about 0 dB in the pass band and 66 dB at the bottom of the skirt.

6. To use the MARKERS functions to read the results of the above measurement directly, proceed as follows:

   a. Press the SOURCE MARKERS key. A menu displays with the M1 marker highlighted.

   b. Use the DATA ENTRY keypad to enter 500 MHz for the M1 marker, then use the rotary knob to position the marker at the end of the passband. The frequency at this point displays opposite "M1." For the above example, instead of being about 500 MHz, it is shown to be exactly 498.91 MHz.

Table 3-1. Making Transmission and Return Loss Measurements (Continued)

c. Read the transmission loss from the "READOUT (M1)" portion of the display. Again for the above example, instead of about 0 dB it is shown to be exactly 0.48 dB.

d. Using the DATA ENTRY rotary knob, move the M1 marker to the bottom of the filter skirt. Read the frequency and power. For the example, the frequency is 734.11 MHz and the transmission loss varies between about -58 and -66 dB.

e. To stop the transmission loss reading from varying, and to provide a more accurate reading, proceed as follows:
   (1) Press the NETWORK ANALYZER SMOOTHING key to light the MAX indicator.
   (2) Press the SOURCE FREQUENCY DATA POINTS key to light the 401 indicator.
   (3) Read the transmission loss as before and note that is much more steady. For the example, it now reads between -61 dB and -65 dB.
   (4) Return SMOOTHING to OFF and FREQUENCY DATA POINTS to 201.

7. Make a hard-copy printout of the transmission loss, as follows:

   a. Press the HARD COPY MENU key.

   b. Select PRINT GRAPH to print the displayed graphic, or select 51, 101, 201, or 401 to print a tabulation at the selected number of frequency points. You could also choose to print out a tabulation at only the marker frequencies, if any markers were on.

   c. Press MENU SELECT or START PRINT to print out the data.

   d. The printout should resemble the one shown in Figure 3-25.

Return Loss Measurement

8. Measure the return loss of the filter, as follows:

   a. Press the Channel A DISPLAY ON/OFF key to off.

   b. Press the Channel B DISPLAY ON/OFF key to on.

   d. Press the Channel B AUTOSCALE key.

9. To use the MARKERS functions to read the results of the above measurement directly, proceed as follows:

   a. Press the SOURCE MARKERS key.

   b. Use the DATA ENTRY rotary knob to read the return loss from any point of interest on the displayed trace. The frequency and return loss values are shown as described in step 6, above.

10. Print out the return loss as described in step 7 above.

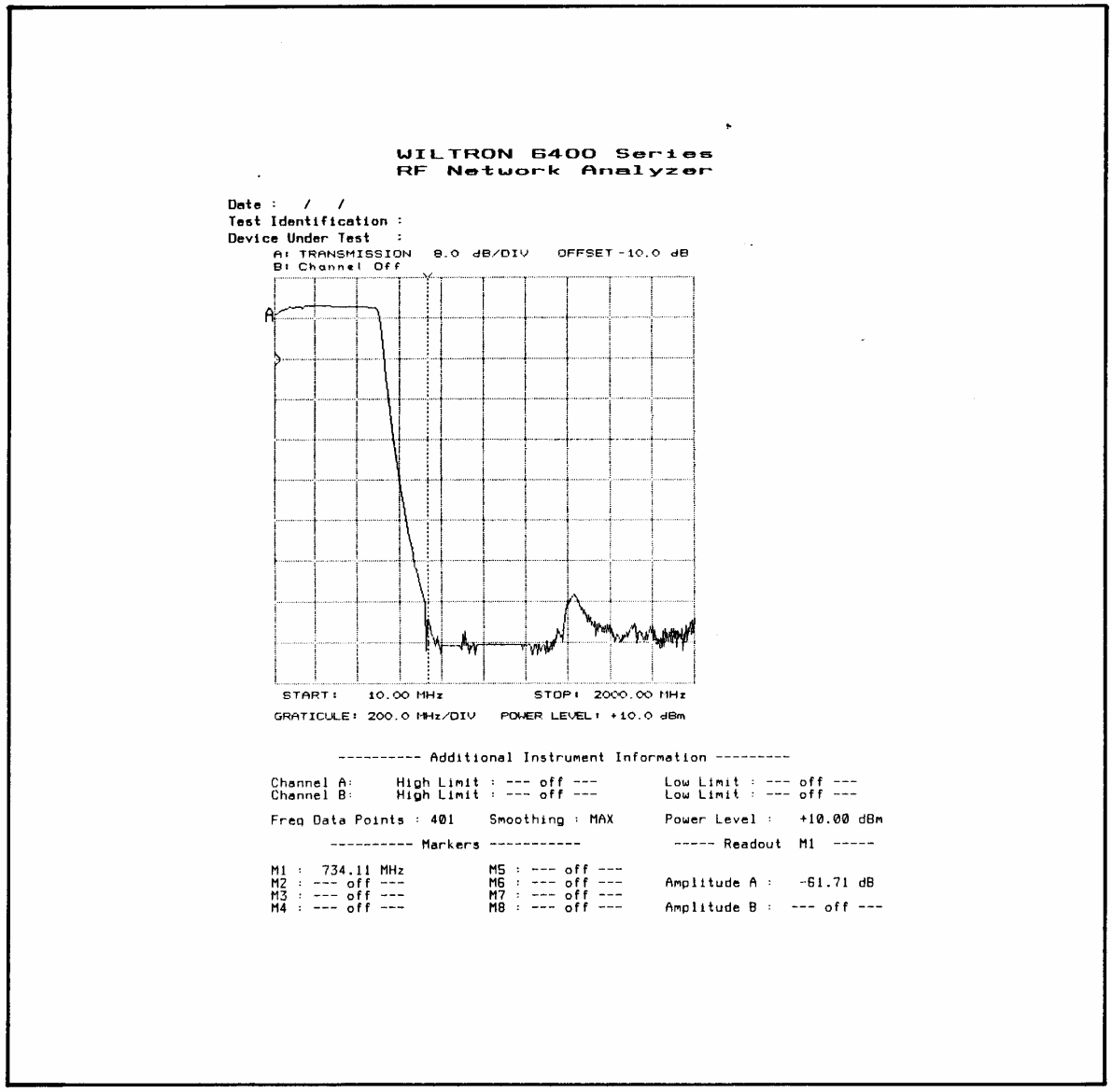


Figure 3-25. Hard-Copy Printout of Displayed Graphic

3-4.2 Absolute Power Measurements

How to make an absolute power measurement is described in Table 3-2.

3-4.3 Alternate Sweep Measurements

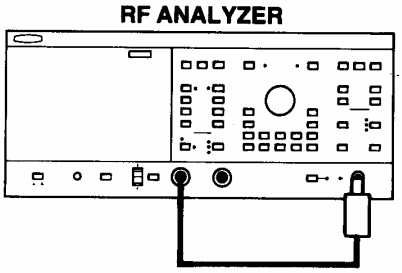
How to make an alternate sweep measurement is described in Table 3-3; a test setup is shown in Figure 3-26.

3-5 OPERATIONAL CHECKOUT

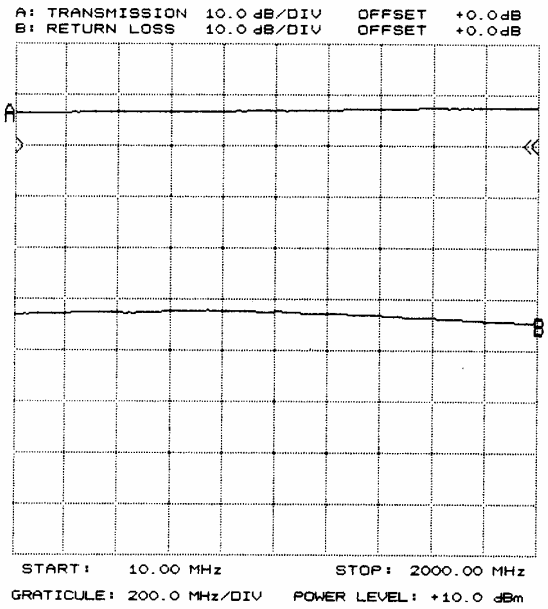
The 6407 and 6409 RF Analyzers undergo a comprehensive self test when turned on or when the RESET or SELF TEST key is pressed. If the CRT displays "ALL TESTS PASSED," the internal circuits are operating properly and the only check needed is source output power. How to perform this check is described in Table 3-4.

Table 3-2. Making an Absolute Power Measurement

1. Connect the RF detector between Connector A and the RF OUTPUT connector, as shown below.



2. Press POWER on the analyzer to on. At the conclusion of the built-in self test, the screen displays "ALL TESTS PASSED," and the CRT resembles that shown below. Control settings may be different from those shown, which are the RESET control settings (6409). The instrument comes on line with the same control setting it had when last turned off.



Screen Display with Factory Selected Control Settings

Table 3-2. Making an Absolute Power Measurement (Continued)

3. Press the Channel B DISPLAY ON/OFF key to off.
4. Press the Channel A MENU key.
5. When the menu appears, select the SET MEASUREMENT TYPE option using the MENU rocker switch and SELECT key.
6. When the next menu appears, select the POWER dBm option using the MENU rocker switch and SELECT key.
7. Press the Channel A AUTOSCALE key. This give an optimum vertical display of the test data.
8. Press the SOURCE MARKERS key.
9. When the menu appears, activate the M1 marker using the DATA ENTRY ENTER key.
10. Using the DATA ENTRY rotary knob, move the marker from the low to the high ends of the trace and read the SOURCE output power, in dBm, at the marker frequency from the READOUT (M1) portion of the screen.

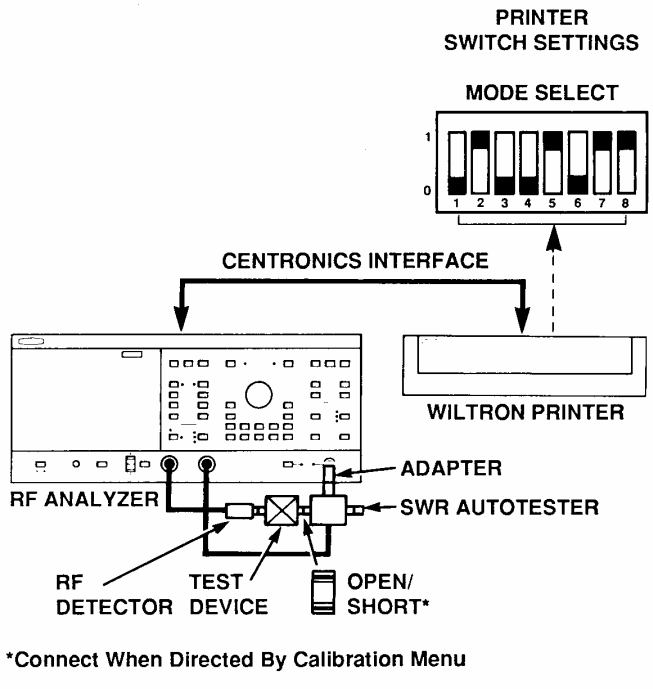
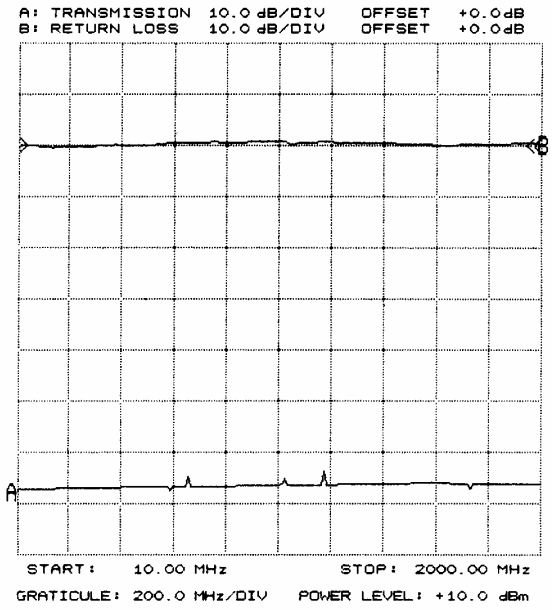


Figure 3-26. Test Setup for Alternate Sweep Measurements

Table 3-3. Making Alternating Sweep Measurements

1. Connect test equipment per Figure 3-26, except do not connect the test device; turn the printer on.

2. Press POWER on the analyzer to on. At the conclusion of the built-in self test, the screen displays "ALL TESTS PASSED," and the CRT resembles that shown below. Control settings may be different from those shown, which are the RESET control settings (6409). The instrument comes on line with the same control settings it had when last turned off. Ensure that both channels are on and that Channel A is set for TRANSMISSION and Channel B for RETURN LOSS.



Screen Display with Factory Selected Control Settings

3. Press the NETWORK ANALYZER CALIBRATION key and follow the directions given in the calibration-cycle sequence of menus. If necessary, refer to Figure 3-9 for an explanation of the menus. After finishing the calibration, connect the test device and RF detector as shown in Figure 3-26.

Transmission Loss Measurement

4. Measure the transmission loss in the Alternating Sweep A mode, as follows:

   a. Press the Channel A AUTOSCALE key. This give an optimum vertical display of the test data.

   b. Press the SOURCE MENU key.

Table 3-3. Making Alternating Sweep Measurements (Continued)

c. **When the menu appears, select the "ALTERNATE, Input A Only" option using the MENU Up/Down switch and SELECT key.**

d. Press the SOURCE FREQUENCY START key.

e. Choose a portion of the displayed trace that you would like to observe in greater detail, then use the DATA ENTRY keypad or rotary knob to enter the ALT START frequency for that portion.

f. **Using the MENU Up/Down switch or the FREQUENCY STOP key, move the menu cursor to the ALT STOP parameter.**

g. Enter a STOP frequency.

h. Press the Channel B AUTOSCALE key.

i. See Figure 3-27 for an example of the Alternating Sweep A mode being used to test a low pass filter.

j. Press the SOURCE MENU key, and select the NORMAL option when the menu appears.

Return Loss Measurement (Channel B)

5. Measure return loss in Alternate Sweep A, B Mode as follows:

a. Press the Channel B AUTOSCALE key.

b. Press the SOURCE MENU key.

c. **When the menu appears, select the ALTERNATE A, B option using the MENU Up/Down switch and SELECT key.**

d. Press the SOURCE FREQUENCY START key.

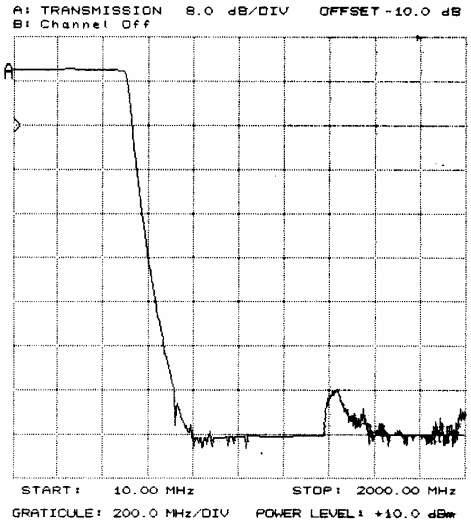
e. Choose a portion of trace B that you would like to observe in greater detail, then use the DATA ENTRY keypad or rotary knob to enter the ALT START frequency.

f. **Select the ALT STOP parameter using the MENU Up/Down switch or the FREQUENCY STOP key.**

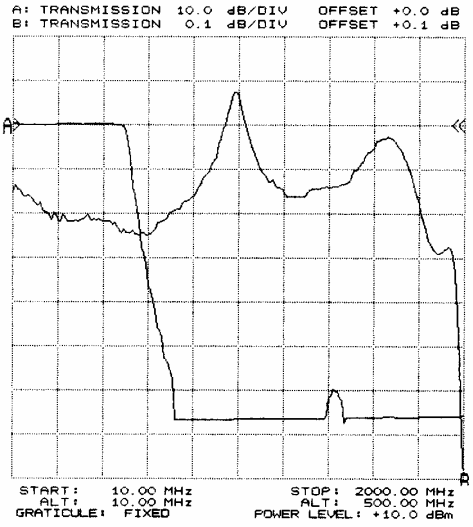
g. Enter a STOP frequency.

h. Press the Channel B AUTOSCALE key.

i. See Figure 3-28 for an example of the Alternating Sweep A, B mode being used to test a low pass filter.

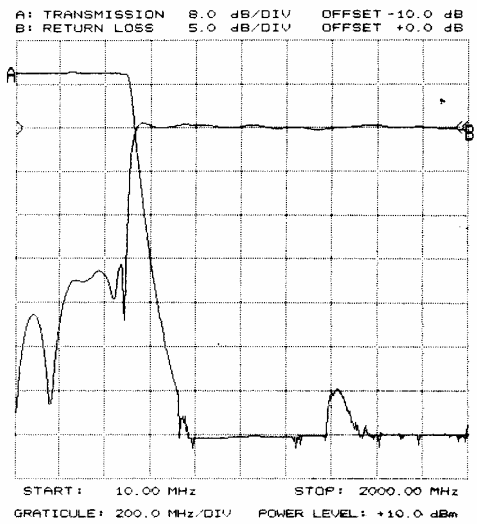


We would like to take a closer look at the pass band on this filter. The pass band starts at 10 MHz and extends to about 500 MHz.

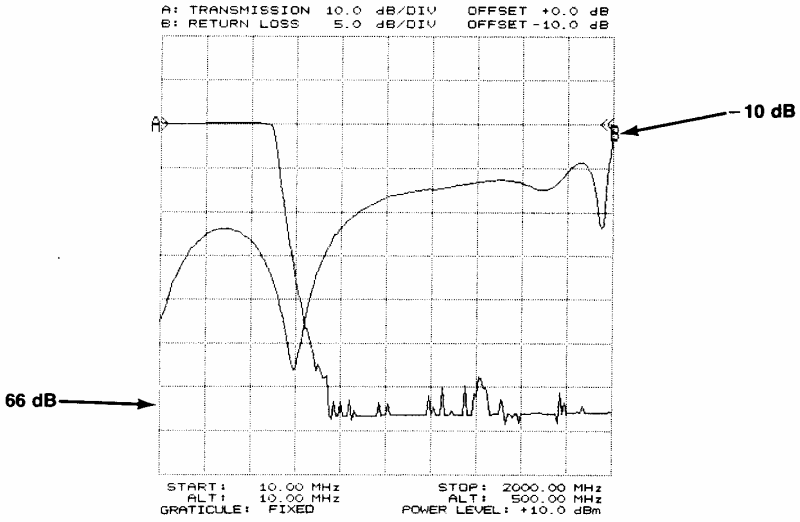


Here is an expanded view of the pass band. The alternate sweep start and stop frequencies are shown opposite "ALT" on the second frequency line, under the GRATICULE crosshatch pattern.

Figure 3-27. Examples of the Alternating Sweep A Measurement of a Low Pass Filter



We would like to take a closer look at return loss of the pass band, which starts at 10 MHz and extends to 500 MHz.

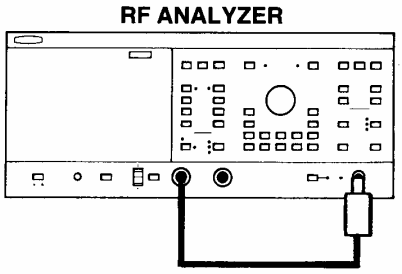


Here is an expanded view of return loss in the pass band, on Trace B. The alternate sweep start and stop frequencies are shown opposite "ALT" on the second frequency line, under the GRATICULE crosshatch pattern. As shown, the highest return loss (closest to 0 dB) is 10 dB (the Trace B reference line is at -10 dB) at 500 MHz, while the lowest return loss is about 66 dB.

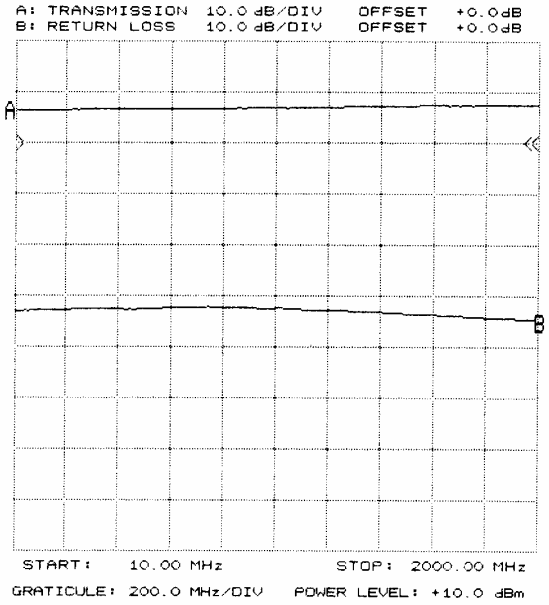
Figure 3-28. Examples of an Alternating Sweep A and B Measurement of a Low Pass Filter

Table 3-4. Operational Checkout Procedure

1. Connect the RF detector between Connector A and the RF OUTPUT connector, as shown below.



2. Press POWER on the analyzer to on. At the conclusion of the built-in self test, the screen displays "ALL TESTS PASSED," and the CRT resembles that shown below. Control settings may be different from those shown, which are the RESET control settings (6409). The instrument comes on line with the same control setting it had when last turned off.



Screen Display with Factory Selected Control Settings

3. Press the Channel B DISPLAY ON/OFF key to off.

Table 3-4. Operational Checkout Procedure (Continued)

4. Press the Channel A MENU key.

5. **When the menu appears, select the POWER dBm option using the MENU Up/Down switch and SELECT key.**

6. When the next menu appears, select the POWER dBm option using the MENU rocker switch and SELECT key.

8. Press the Channel A OFFSET/RESOLUTION key.

9. When the menu appears, select the OFFSET option and enter the following using the DATA ENTRY keypad or rotary knob:
   a. 6407/6409 with 50Ω output: 10 dB .
   b. 6407 with 75Ω output: 8 dB

10. Select the RESOLUTION option and enter 2 dB using the DATA ENTRY keypad or rotary knob.

11. Press the SOURCE POWER LEVEL key.

12. Enter a new power level as follows, using the DATA ENTRY keypad or rotary knob.
   a. 6407/6409 with 50Ω output: 2 dB .
   b. 6407 with 75Ω output: 0 dB

13. Observe that the trace deflects downward by 4 divisions.

3-6 ERROR MESSAGES

Upon turning on the equipment or pressing the SELF TEST or RESET keys, the RF analyzer undergoes a comprehensive self test. If the self test passes, the message "ALL TESTS PASSED" displays; however, if any part of the self test fails, an error message displays instead. In addition, a control panel LED flashes. A different LED flashes for each fault. The LED coding for fault detection is shown in Table 3-5. This coding makes it possible to locate a fault even if the CRT has failed.

Table 3-5. Control Panel LED Error Codes

FLASHING LED	FAULT	FAULT LOCATION
FREQUENCY DATA POINTS 401	RAM	A6 Microprocessor PCB
SMOOTHING OFF	ROM	A6 Microprocessor PCB
FREQUENCY DATA POINTS 201	TICK*	A9 Power Supply PCB and/or A10 Motherboard PCB
FREQUENCY DATA POINTS 101	Stuck Switch	A1 Main Control Panel PCB
CALIBRATE BEGIN	Control Panel, other than stuck switch.	A1 Main Control Panel PCB or A11 Subsidiary Control Panel PCB
UNCALIBRATED	Stuck Graphic Display Processor (GDP) Handshake	A7 GDP PCB
SMOOTHING MAX	No GDP Handshake	A7 GDP PCB
SMOOTHING MIN	No Analog-to-Digital Conversion	A3 Signal Channel PCB
DISPLAY A ON/OFF	Partial Autozero Failure	A3 Signal Channel PCB
DISPLAY B ON/OFF	No Markers	A4 Sweeper PCB or RF Deck
RF ON/OFF	Stuck Markers	A4 Sweeper PCB or RF Deck
REMOTE	Total Autozero Failure	A3 Signal Channel PCB
HOLD	Warning that Probes are Missing	None

*TICK is the name of an internal timing pulse that is derived from the line frequency (50 or 60 Hz). This pulse synchronizes the graphic display oscillator and prevents the displayed image from "wobbling."

SECTION IV
REMOTE (GPIB) OPERATION

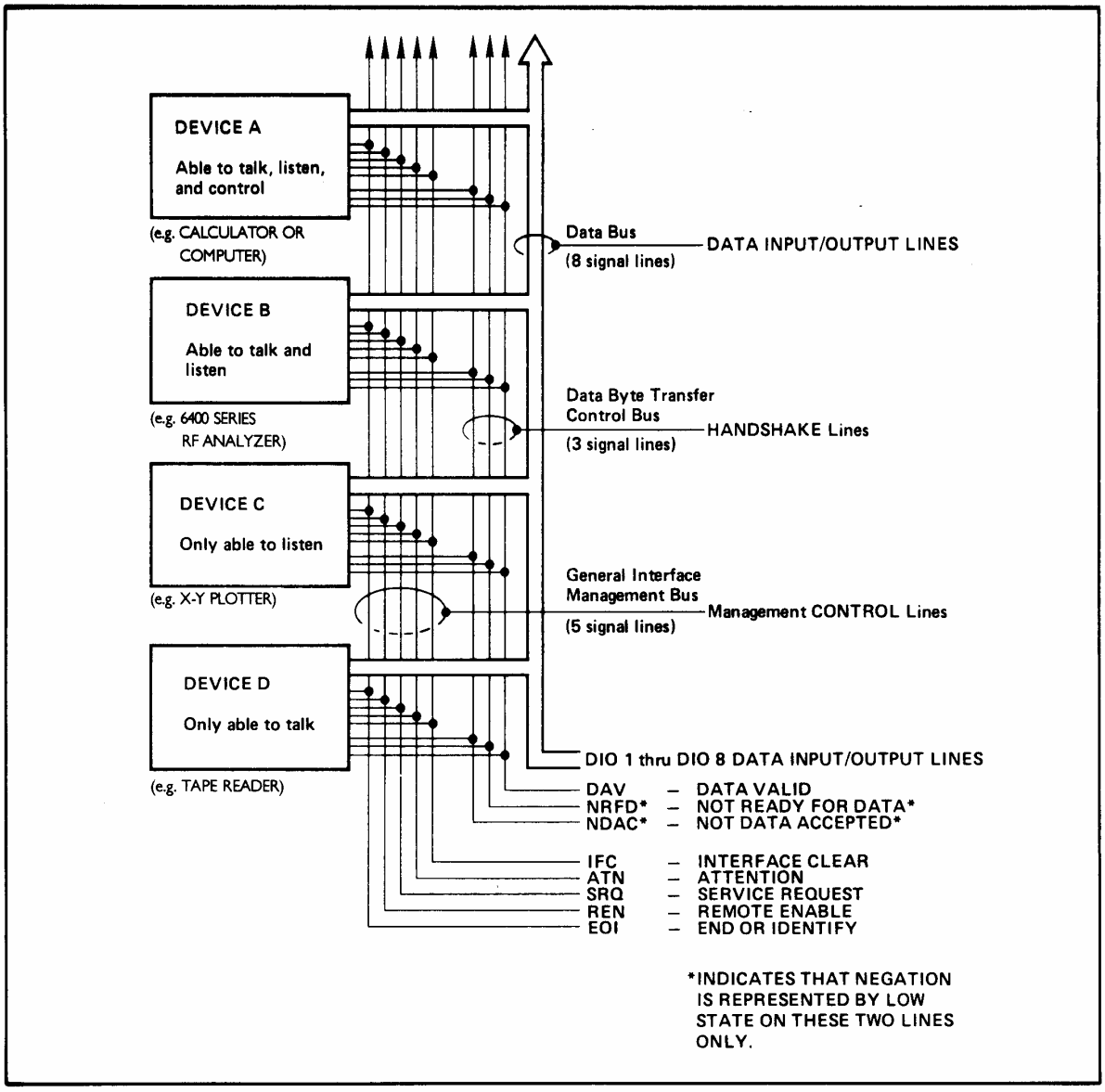


Figure 4-1. Interface Connections and Bus Structure

SECTION IV
REMOTE (GPIB) OPERATION

4-1 INTRODUCTION

This section provides a description of the GPIB and the RF analyzer command codes. It also provides several examples of bus programming.

4-2 DESCRIPTION OF THE IEEE-488 INTERFACE BUS

The IEEE-488 bus (General Purpose Interface Bus--GPIB) is an instrumentation interface for integrating instruments, calculators, and computers into systems. The bus uses 16 signal lines to effect transfer of data and commands to as many as 15 instruments.

The instruments on the bus are connected in parallel, as shown in Figure 4-1 on the facing page. Eight of the signal lines (DIO 1 thru DIO 8) are used for the transfer of data and other messages in a byte-serial, bit-parallel form. The remaining eight lines are used for communications timing (handshake), control, and status information. Data are transmitted on the eight GPIB data lines as a series of eight-bit characters, referred to as bytes. Normally, a seven-bit ASCII (American Standard Code for Information Interchange) code is used. The eighth (parity) bit is not used. Data transferral is by means of an interlocked handshake technique.

This technique permits asynchronous communications over a wide range of data rates. The following paragraphs provide an overview of the data, management, and handshake buses, and describe how these buses interface with the RF analyzer.

4-2.1 Data Bus Description

The data bus is the conduit for transmitting control information and data between the controller and the RF analyzer. It contains eight bi-directional, active-low signal lines--DIO 1 thru DIO 8. One byte of information (eight bits) is transferred over the bus at a time. DIO 1 represents the least-significant bit (LSB) in this byte and DIO 8 represents the most-significant bit (MSB). Each byte represents a peripheral address (either primary or secondary), a control word, or a data byte. Data bytes are usually formatted in ASCII code, without parity.

4-2.2 Management Bus Description

The management bus is a group of five signal lines used to control the operation of the bus system. Functional information regarding the individual control lines is provided below.

a. ATN (attention). When TRUE, the RF analyzer responds to appropriate interface messages--such as, device clear and serial poll--and to its own listen/talk address.

b. EOI (end or identify). When TRUE, the last byte of a multibyte message has been placed on the line. Also used in conjunction with ATN to indicate a parallel poll.

c. IFC (interface clear). When TRUE, the RF analyzer interface functions are placed in a known state--such as, unaddressed to talk, unaddressed to listen, and service request idle.

d. REN (remote enable). When TRUE the RF analyzer is enabled--upon receipt of its listen address--for entry into the remote state. The mode is exited either when the REN line goes FALSE (high) or when the RF analyzer receives a go-to-local (GTL) message.

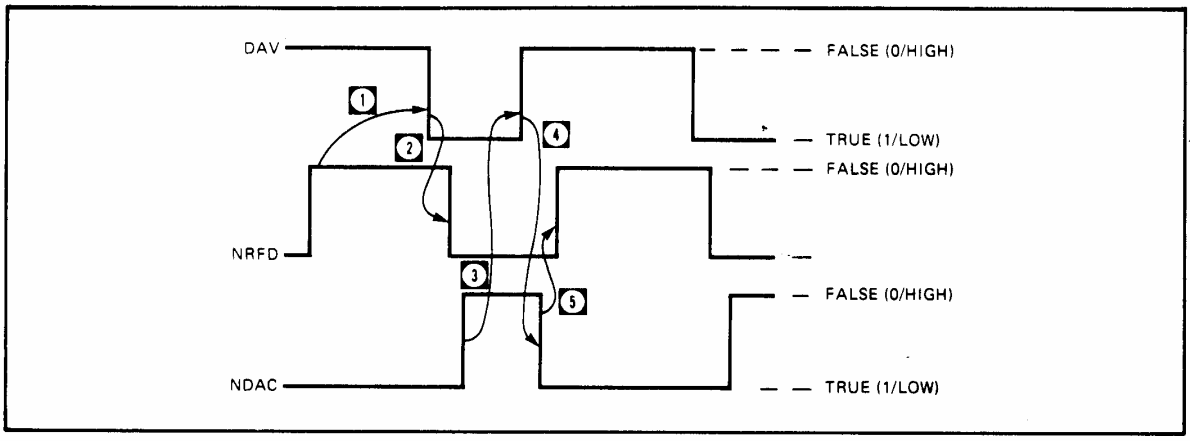


Figure 4-2. Typical Handshake Operation

e. SRQ (service request). This line is pulled LOW (true) by the RF analyzer to indicate that certain preprogrammed conditions exist.

4-2.3 Data Byte Transfer Control (Handshake) Bus Description

Information is transferred on the data lines by a technique called the three-wire handshake. The three handshake-bus signal lines (Figure 4-2) are described below.

a. DAV (data valid). Goes TRUE (arrow 1) when the talker has (1) sensed that NRFD is FALSE, (2) placed a byte of data on the bus, and (3) waited an appropriate length of time for the data to settle.

b. NRFD (not ready for data). Goes TRUE (arrow 2) when a listener indicates that valid data has not yet been accepted. The time between the events shown by arrows 1 and 2 is variable and depends upon the speed with which a listener can accept the information.

c. NDAC (not data accepted). Goes FALSE to indicate that a listener has accepted the current data byte for internal processing. When the data byte has been accepted, the listener releases its hold on NDAC and allows the line to go FALSE. However since the GPIB is constructed in a wired-OR configuration, NDAC will not go FALSE until all listeners participating in the interchange have also released the line. As shown by arrow 3, when NDAC goes FALSE, DAV follows suit a short time later. The FALSE state of DAV indicates that valid data has been removed; consequently, NDAC goes LOW in preparation for the next data interchange (arrow 4).

Arrow 5 shows the next action in time: NRFD going FALSE after NDAC has returned TRUE. The FALSE state of NRFD indicates that all listeners are ready for the next information interchange. The time between these last two events is variable and depends on how long it takes a listener to process the data byte. In summation, the wired-OR construction forces a talker to wait for the slowest instrument to accept the current data byte before placing a new data byte on the bus.

4-3 GPIB OPERATION

All front panel keys, except for POWER are bus controllable. When used on the GPIB, the RF analyzer functions as both a listener and a talker. Table 4-1 provides a listing of the GPIB subset functions.

4-4 COMMAND CODES, DESCRIPTIONS

The command codes recognized by the RF analyzer are divided into Control Panel Key, SRQ, and Display-Read Codes. They are described in the following Tables 4-2 thru 4-4.

4-5 BUS MESSAGES, RF ANALYZER RESPONSE TO

Table 4-5 lists the bus messages responded to by the RF analyzer. Table 4-6 lists programming statements showing how the WILTRON 85 and HP Series 200 bus controllers implement the recognized bus messages.

4-6 ALPHABETICAL INDEX TO RF ANALYZER COMMAND CODES

Table 4-7 lists an alphabetical index to the 6407 and 6409 RF Analyzer Command Codes.

Table 4-1. 6400 Series IEEE-488 Bus Subset Capability

GPIB SUBSET	FUNCTION	DESCRIPTION	GPIB SUBSET	FUNCTION	DESCRIPTION
AH1	Acceptor Handshake	Complete Capability	SR1	Service Request	Complete Capability
SH1	Source Handshake	Complete Capability	RL1	Remote/ Local	Complete Capability
T6	Talker	No Talk Only (TON)	PP1	Parallel Poll	Complete Capability
TE0	Talker With Address Extension	No Capability	DC1	Device Clear	Complete Capability
L4	Listener	No Listen Only (LON)	DT1	Device Trigger	No Capability
LE0	Listener With Address Extension	No Capability	C1, C2 C3, C28	Controller	No Capability

Table 4-2. Control Panel Command Codes (1 of 7)

COMMAND CODE	MNEMONIC	FUNCTION
	Network Analyzer, Channel/Trace A	
AP	Channel A to Power	Turns on RF analyzer and configures Channel A to measure and Trace A to display absolute power in dBm.
AT	Channel A to Transmission	Turns on RF analyzer and configures Channel A to measure and Trace A to display transmission loss or gain.
AR	Channel A to Return Loss	Turns on RF analyzer and configures Channel A to measure and Trace A to display return loss.
ACL	Channel A to CaLibration	Turns on RF analyzer and configures Trace A to display the calibration data stored in memory.
AS	Trace A Select	Switches Trace A off and on. Programming "AS /" turns the trace off and "AS *" turns it on again. The trace comes back on in the same mode (TRANSMISSION, RETURN LOSS, POWER, CAL DATA) as when turned off last.
AA	Channel A Autoscale	Selects automatic scaling of the Channel A measurement data displayed on Trace A.
AOF	Trace A OFfset	Sets the offset value for Trace A. For example, programming "AOF -10" sets Trace A offset at -10 dB.
ADD	Trace A resolution in dB per Division	Sets the vertical resolution of Trace A. For example, programming "ADD 10" sets the Trace A resolution for 10 dB per division.
AH	Trace A High Limit Line	Sets the value for or turns the Trace A high limit line on or off. For example, programming "AH -10" sets the limit line at -10 dB, "AH /" turns the line off, and "AH *" turns it on.
AL	Trace A Low Limit Line	Sets the value for or turns the Trace A low limit line on and off. For example, programming "AH -10" sets the limit line at -10 dB, "AH /" turns the line off, and "AH *" turns it on.

Table 4-2. Control Panel Command Codes (2 of 7)

COMMAND CODE	MNEMONIC	FUNCTION
	Network Analyzer, Channel/Trace A (Continued)	
ADR 0 thru ADR 10	Trace A Display Reference	Selects on which graticule line the Trace A reference line is to appear. For example, programming "ADR 0" places the reference on the top graticule line and "ADR 10" places it on the bottom graticule line.
	Network Analyzer, Channel/Trace B	
The Channel/Trace B command codes are the same as those for Channel/Trace A, except use "B" instead of "A" for the first letter. That is, use "BP,""BT,""BR," etc. instead of "AP,""AT,"AR," etc.		
	Network Analyzer, Smoothing	
SOF	Smoothing OFf	Sets smoothing (low-level filtering) to off.
SIN	Smoothing mINimum	Sets smoothing to minimum.
SAX	Smoothing mAXimum	Sets smoothing to maximum.
	Network Analyzer Calibration	
CAL	CALibrate	Initiates a measurement calibration sequence. The calibration menus (Figure 3-9 on page 3-5) are displayed on the RF analyzer. (The command suppresses the GPIB status menu on the RF analyzer CRT.) The SELECT key on the RF analyzer is inoperative; its function is replaced by the CON command (below).
CON	CONtinue	Calls up the next calibration menu. That is, after completing the instructions given in the calibration menu, send "CON" instead of pressing SELECT. The RF analyzer will respond to "CON" so long as the number-6 character in the Read Status ASCII string is a question mark (?). See Figure 4-3 on page 4-13.

Table 4-2. Control Panel Command Codes (3 of 7)

COMMAND CODE	MNEMONIC	FUNCTION
		NOTE It is important to monitor the RS command "Calibrate in Progress" character during the calibration operation. If the RF analyzer returns an "M," it has aborted the calibration sequence. An "M" is returned if 1. neither channel/trace was set to TRANSMISSION nor RETURN LOSS, 2. the RF has been switched off, 3. the RF analyzer is in the "Alternate A" or "Alternate A or B" mode, 4. the RF analyzer is in the "Hold" mode.
		Frequency Source, Sweep Functions
SSM	Sweep Standard Mode	Sets the source for the normal, non-alternating, sweep mode.
SAA	Sweep Alternate A mode	Sets the source for the Alternate A sweep mode. Refer to Figure 3-19 on page 3-11 for a description of this mode.
SAB	Sweep Alternate A/B mode	Sets the source for the Alternate A/B sweep mode.
ST	Sweep StarT Frequency	Sets the sweep start frequency in MHz. For example, programming "ST 10" sets the sweep to start at 10 MHz.
SP	Sweep StoP Frequency	Sets the sweep stop frequency in MHz. For example, programming "SP 2000" sets the sweep to stop at 2000 MHz.
SC	Sweep Center Frequency	Sets the sweep center frequency in MHz. For example, programming "SC 1000" sets the sweep center frequency to 1000 MHz. Used in conjunction with the SW code on the next page this code sets the center-frequency value for a ΔF sweep (a sweep that is symmetrical about a center frequency).

Table 4-2. Control Panel Command Codes (4 of 7)

COMMAND CODE	MNEMONIC	FUNCTION
SW	Sweep Width Frequency	Sets the width for a ΔF sweep in MHz, when used with the SC code on the preceeding page. For example, programming "SW 500" sets the ΔF sweep width for 500 MHz. In this example, 500 MHz, the sweep starts 250 MHz below the center frequency (Fc) and sweeps to 250 MHz above Fc.
SAT	Sweep Alternate StarT Frequency	Sets the alternate sweep start frequency in MHz. For example, programming "SAT 10" sets the alternate sweep to start at 10 MHz. Refer to Figure 3-19 on page 3-11 for a description of the alternate sweep mode.
SAP	Sweep Alternate StoP Frequency	Sets the alternate sweep stop frequency in MHz. For example, programming "SAP 2000" sets the alternate sweep to stop at 2000 MHz.
SAC	Sweep Alternate Center Frequency	Sets the alternate sweep center frequency. in MHz. For example, programming "SAC 1000" sets the alternate sweep center frequency to 1000 MHz. Used in conjunction with the SAW code below, this code sets the center frequency for an alternate ΔF sweep; that is, a sweep that is symmetrical about a given frequency.
SAW	Sweep Alternate Width	Sets the alternate sweep width in MHz, when used with the SAC code above. For example, programming "SAW 500" sets the alternate sweep width for 500 MHz. For this example, 500 MHz, the sweep starts 250 MHz below the center frequency (Fc) and stops 250 MHz above Fc.
SFB	Sweep Full Band	Sets the source for a full-band sweep; that is, 1 MHz to 1000 MHz for the 6407 and 10 MHz to 2000 MHz for the 6409.

Table 4-2. Control Panel Command Codes (5 of 7)

COMMAND CODE	MNEMONIC	FUNCTION
	Frequency Source, Marker Functions	
FM	Frequency Markers	Display all frequency markers or only the active (readout) frequency marker. For example, programming "FM *" displays all frequency markers on the RF analyzer CRT and "FM /" displays only the active marker.
M1 thru M8	Markers M1 thru M8	Selects one of the M1 thru M8 markers to be active and sets its frequency in MHz. Also turns the active marker on or off. For example, programming "M1 1000" selects M1 as the active marker and sets it to 1000 MHz. Programming "M1 /" turns the M1 marker off and "M1 *" turns it on again.
	Frequency Source, Power Level Function	
PWR	PoWeR	Sets the output power level in dBm, and turns the RF output on and off. For example, programming "PWR .2" sets the output power level for 0.2 dBm, and programming "PWR /" turns the RF off and "PWR *" turns it on again.
	Frequency Source, Marker Readout Function	
RAM 1 thru RAM 8	Read Trace A Marker 1 thru Marker 8	Configures the 6400 to read and return the value of Trace A at the specified marker, when addressed to talk. For example, programming RAM 3 makes marker 3 the readout (active) marker and returns the amplitude of the trace, in dB, at this frequency. Only the amplitude is returned, not the frequency.
RBM 1 thru RBM 8	Read Trace B Marker 1 thru Marker 8	Configures the 6400 to read and return the value of Trace B at the specified marker, when addressed to talk. For example, programming RBM 3 makes marker 3 the readout (active) marker and returns the amplitude of the trace, in dB, at this frequency. Only the amplitude is returned, not the frequency.

Table 4-2. Control Panel Command Codes (6 of 7)

COMMAND CODE	MNEMONIC	FUNCTION
	Hard Copy Function	
PG	Print Graph	Provides a hard-copy printout on the companion printer of the graph displayed on the CRT.
T02	Tabulation at 26 Points	Provides a hard-copy tabulation at 26 frequencies on the companion printer.
T05	Tabulation at 51 Points	Provides a hard-copy tabulation at 51 frequencies on the companion printer.
T10	Tabulation at 101 points	Provides a hard-copy tabulation at 101 frequencies on the companion printer.
T20	Tabulation at 201 points	Provides a hard-copy tabulation at 201 frequencies on the companion printer.
T40	Tabulation at 401 points	Provides a hard-copy tabulation at 401 frequencies on the companion printer.
TMO	Tabulation at Marker Frequencies Only	Provides a hard-copy tabulation only at the marker frequencies on the companion printer.
HP	Halt Printing	Immediately halts the printing of data and clears the print buffer.
	Graticule On/Off Function	
GR	GRatical	Turns the CRT graticule on and off. When off, the CRT displays tick marks. For example, programming "GR *" turns the graticule on and "GR /" turns it off.
	Reset Function	
RES	RESet	Resets the control panel with the factory-selected settings shown in paragraph 3-2.2c on page 3-3. Calibration data are not affected.
	Save/Recall Control Panel Setups Function	
PSS1 thru PSS9	Panel Setup Save in Memory	Saves the current control panel setup in one of the nine memory locations. For example, programming "PSS 8" saves the present control panel setup in memory location 8.

Table 4-2. Control Panel Command Codes (7 of 7)

COMMAND CODE	MNEMONIC	FUNCTION
	Save/Recall Control Panel Setups Function (Continued)	
PSR1 thru PSR9	Panel Setup Recall from Memory	Recalls the control panel setup stored in the numbered memory location back to the control panel. For example, programming "PSR 8" recalls the control panel setup previously stored in memory location 8.
	Self Test Function	
TST	Self TeST	Runs the built-in self test. If the "ALL TESTS PASSED" notation displays on the RF analyzer, then the RF analyzer will respond to commands from the GPIB. If the RF analyzer fails self test, it will not respond to GPIB programming--only to control panel keys.
	Hold Function	
HLD	HoLD	Holds or releases current measurement data. For example, programming "HLD *" holds the data and "HLD /" releases it.
FDP1	Frequency Data Points to 101	Sets the frequency axis to 101 data points.
FDP2	Frequency Data Points to 201	Sets the frequency axis resolution of display to 201 data points.
FDP4	Frequency Data Points to 401.	Sets the frequency axis resolution of display to 401 data points.

Table 4-3. Service Request (SRQ) Command Codes

COMMAND CODE	MNEMONIC	FUNCTION
SQS n	SRQ After a Number of Sweeps	Generates an SRQ bus message after the "n" number of sweeps have occurred. For example, programming "SQS 25" generates an SRQ message after 25 sweeps.
Q 0 thru Q 4	SRQ Select	Enables or disables the indicated bit in the status-byte mask. For example, programming "Q 2 *" enables bit 2, while "Q 0 /" disables bit 0. The status-byte bits are shown in below.

STATUS BYTE

NOT IMPLEMENTED Bit 7	SRQ Bit 6	NOT IMPLEMENTED Bit 5	END OF HARD-COPY OPERATION Bit 4	END OF CALIBRATION SEQUENCE Bit 3	WARNING CONDITION HAS OCCURRED Bit 2	ERROR CONDITION HAS OCCURRED Bit 1	PROGRAMMED NUMBER OF SWEEP COMPLETED Bit 0

Table 4-4. Display and Read Command Codes (1 of 2)

COMMAND CODE	MNEMONIC	FUNCTION
		Display Codes
DS	DiSplay Area Control	Blanks and unblanks the RF analyzer CRT. For example, programming "DS /" blanks the CRT and "DS *" unblanks it. DS* is the default condition.
DMR	Display Marker Readout	Displays GPIB status or active (readout) marker dB values on the RF analyzer CRT. For example, programming "DMR *" displays the active marker status and "DMR /" the GPIB status. DMR/ is the default condition.
		Read Codes
RS	Read Status	Configures the 6400 to read and return the current status of the RF analyzer. This status information is returned as a string of nine ASCII characters. See Figure 4-3 for a description of the status information.
RP 1 thru RP34	Read Parameter	Configures the 6400 to read and return parameter values, with each parameter being uniquely identified by a number from 1 to 34 (see below). For example, programming "RP 1" returns the Trace A offset value and "RP 34" the dB value of the active (readout) marker on Trace B.

No.	Parameter
1	Trace A Offset in dB
2	Trace B Offset in dB
3	Trace A Resolution in dB/Division
4	Trace B Resolution in dB/Division
5	Trace A High Limit in dB
6	Trace A Low Limit in dB
7	Trace B High Limit in dB
8	Trace B Low Limit in dB
9	Sweep Start Frequency in MHz
10	Sweep Stop Frequency in MHz
11	Sweep Center Frequency in MHz
12	Sweep Width in MHz
13	Not Used
14	Marker 1 Frequency in MHz
15	Marker 2 Frequency in MHz
16	Marker 3 Frequency in MHz
17	Marker 4 Frequency in MHz
18	Marker 5 Frequency in MHz

Table 4-4. Display and Read Command Codes (Continued)

COMMAND CODE	MNEMONIC	FUNCTION
		Read Codes (Continued)
RP 0 thru RP 34 (Cont)	Read Parameter	Parameter Numbers (Continued) **No. Parameter** 17 Marker 4 Frequency in MHz 18 Marker 5 Frequency in MHz 19 Marker 6 Frequency in MHz 20 Marker 7 Frequency in MHz 21 Marker 8 Frequency in MHz 22 Not Used 23 Output Power Level in dBm 25 ALT Sweep Start Frequency in MHz 26 ALT Sweep Stop Frequency in MHz 27 ALT Center Frequency in MHz 28 ALT Sweep Width in MHz 29 Not Used 30 Not Used 31 Graticule Value in MHz/Division 32 Value of Number-of-Sweeps Counter 33 dB Value of Trace A Active Marker 34 dB Value of Trace B Active Marker
RATxx RBTxx	Read A Trace Read B Trace	Configures the 6400 to convert the trace on the screen into a set of numbers. These numbers are then transferred from the 6400 to the HP85 in the form of a block of ASCII characters made up of a + or - sign, two digits, a decimal point, then two more digits (e.g. -37.52). A trace representative of that observed on the 6400 screen can then be printed out on the HP85. "xx" equals the number of data points to be sent over the bus to the computer. For example, RAT02 = 26 data points transferred RAT05 = 51 data points transferred RAT10 = 101 data points transferred RAT20 = 201 data points transferred RAT40 = 401 data points transferred

The current status of the RF analyzer is returned to the controller in a nine-character-long ASCII string, with each character being a four-bit byte. The codes for each of these nine ASCII characters are as follows:

Character	Name	Code
1	Current Error/ Warning	Number from "0" to "8" that identifies the latest Error or Warning message to appear in the message area of the CRT. An Error/Warning Code is updated by a further Error/Warning or cleared by a "Return to Local".

	Code	Message
	0	Clear
Error	1	Entry Error
Error	3	No Cal data
Warning	4	Cal data taken at different pwr
Warning	6	Start/stop or width too wide
Warning	8	Wrong Cal data

Codes 2, 5, 7, and 9 are not supported and will never occur.

2	Previous Error/ Warning	Number from "0" to "8" that identifies Errors/Warning messages that previously appeared in the message area of the CRT. The code is updated by a further Error/Warning occuring or cleared by a "Return to Local".
3	Calibrated/ Uncalibrated	The letter "U" signifies the measurement is uncalibrated, while "C" signifies it is calibrated.
4	Valid Data on Trace A	The letter "V" signifies the measurement data on Trace A are valid, while a "?" signifies they are invalid.
5	Valid Data on Trace B	The letter "V" signifies the measurement data on Trace B are valid, while a "?" signifies they are invalid.
6	Calibration in Progress	The "?" signifies a calibration sequence is in progress, while an "M" signifies completion.
7	Reserved	
8	Sweep Counter	Number from "0" to "9" identifies the number of sweeps that have occured since the counter was set.
9	Printing	The letter "P" signifies the data is being printed, while "M" signifies that no printout is in progress.

Figure 4-3. Read-Status Codes for ASCII Characters

Table 4-5. Bus Messages Recognized by the 6407 and 6409 RF Analyzers (1 of 2)

BUS MESSAGES	HOW MESSAGE IS USED BY THE RF ANALYZER
Device Clear	Resets the RF analyzer to its default state. Sending this message is equivalent to sending the RES command.
Go to Local	Returns the RF analyzer to local (control panel) control.
Group Execute	No action.
Interface Clear	Stops the RF analyzer GPIB interface from listening or talking. The control panel controls are not cleared, however.
Local Lockout	Prevents the front panel RETURN TO LOCAL key from returning the RF analyzer to local (control panel) control.
Remote Enable	Places the RF analyzer under remote (GPIB) control if the REM line is TRUE and the RF analyzer has been addressed to listen. NOTE If the RF analyzer is placed in remote and not supplied with program data, its operation is determined by the positions in which the front panel controls were set immediately prior to going remote.
Service Request Messages	The RF analyzer has been equipped with an SRQ capability. It will respond to both serial- and parallel-poll messages. Responses to these messages are described below.
Serial-Poll Enable (SPE)	The SPE message causes the RF analyzer to respond with a decimally-coded status byte (Table 4-3). This status byte is coded to tell whether it asked for service and, if so, what type of service it needs.
Serial-Poll Disable (SPD)	The SPD message, which the controller sends, terminates a serial poll operation. Parallel Poll Operation When queried by a parallel-poll message (PPOLL, Table 4-6), the RF analyzer (if configured for parallel-poll operation) responds by setting its assigned data bus line to the logical state (1, 0) that indicates its correct SRQ status. To configure a bus device that is (1) built for parallel-poll operation and (2) designed to be remotely configured via the bus, the controller sends a two-byte parallel-poll configure and enable (PPC and PPE) message.

Table 4-5. Bus Messages Recognized by the 6407 and 6409 RF Analyzers (2 of 2)

BUS MESSAGES	HOW MESSAGE IS USED BY THE RF ANALYZER
Parallel-Poll Configure (PPC)	The PPC byte configures the device to respond to a parallel-poll message, such as PPOLL.
Parallel-Poll Enable (PPE)	The PPE byte assigns the logical sense (1, 0) that the parallel-poll response will take. When the RF analyzer receives the PPC/PPE message, it configures itself to properly respond to the parallel-poll message.
Parallel-Poll Unconfigure (PPU)	The PPU (or PPD) message is sent by the controller when a parallel-poll response is no longer needed. This message causes the RF analyzer to become unconfigured for a parallel-poll response.
Parallel-Poll Disable (PPD)	

Table 4-6. Methods of Generating Bus Commands

FUNCTION	METHOD OF EXECUTION	
	WILTRON 85	HP SERIES 200
Go to Local (GTL)	LOCAL 5* LOCAL 705	LOCAL 5 LOCAL 705
Interface Clear (IFC)	ABORTIO 5	ABORT 5
Device Clear (DC) (SDC)	CLEAR 5 CLEAR 705	CLEAR 5 CLEAR 705
Local Lockout (LLO)	LOCAL LOCKOUT 5	LOCAL LOCKOUT 5
Remote Enable (REN)	REMOTE 5 REMOTE 705	REMOTE 5 REMOTE 705
Serial Poll	A=SPOLL (705)	A=SPOLL (705)
Parallel Poll Configure (PPC)	SEND 7; UNL LISTEN 5 CMD 3 SCG 5	PPOLL CONFIGURE 705; 4
Parallel Poll	A=PPOLL (5)	A=PPOLL (5)
Parallel Poll Unconfigure (PPU)	SEND 7; CMD 21 SEND 7; UNL LISTEN 5 CMD 21	PPOLL UNCONFIGURE 7 PPOLL UNCONFIGURE 705

* Assumes GPIB address set to 5.

Table 4-7. Alphabetical Index of RF Analyzer Command Codes (1 of 2)

COMMAND CODE	NAME	TABLE NUMBER
	A	
AA	Channel A Autoscale	4-2
ACL	Trace A to Calibration	4-2
ADD	Trace A Resolution dB/Div	4-2
ADR	Trace A Reference	4-2
AH	Trace A High Limit Line	4-2
AL	Trace A Low Limit Line	4-2
AOF	Trace A Offset	4-2
AP	Channel A to Power	4-2
AR	Channel A to Return Loss	4-2
AS	Trace A Select	4-2
AT	Channel A to Transmission	4-2
	B	
BA	Channel B Autoscale	4-2
BCL	Trace B to Calibration	4-2
BDD	Trace B Resolution dB/Div	4-2
BDR	Trace B Reference	4-2
BH	Trace B High Limit Line	4-2
BL	Trace B Low Limit Line	4-2
BOF	Trace B Offset	4-2
BP	Channel B to Power	4-2
BR	Channel B to Return Loss	4-2
BS	Trace B Select	4-2
BT	Channel B to Transmission	4-2
	C, D	
CAL	Calibrate Trace	4-2
CON	Continue	4-2
DMR	Display Marker Readout	4-4
DS	Display Area Control	4-4
	F, G, H	
FM	Frequency Markers	4-2
GR	Graticule On/Off	4-2
HLD	Hold	4-2
HP	Halt Printing	4-2
	M	
M1-M8	Markers M1 thru M8	4-2
	P,Q	
PG	Print Graph	4-2
PSR	Panel Setup Recall	4-2
PSS	Panel Setup Save	4-2
PWR	Output Power	4-2
Q	SRQ Select	4-3
	R	
RAM	Read Trace A Marker	4-2
RBM	Read Trace B Marker	4-2
RAT	Read A Trace	4-2
RBT	Read B Trace	4-2
RES	Reset	4-2
RP	Read Parameter	4-4
RS	Read Status	4-4
	S	
SAA	Sweep Alternate A Mode	4-2
SAB	Sweep Alternate B Mode	4-2
SAC	Sweep Alternate Center Frequency	4-2
SAP	Sweep Alternate Stop Frequency	4-2
SAT	Sweep Alternate Start Frequency	4-2
SAW	Sweep Alternate Width	4-2
SC	Sweep Center Frequency	4-2

Table 4-7. Alphabetical Index of RF Analyzer Command Codes (2 of 2)

COMMAND CODE	NAME	TABLE NUMBER
	S (Cont)	
SAX	Smoothing Maximum	4-2
SFB	Sweep Full Band	4-2
SIN	Smoothing Minimum	4-2
SOF	Smoothing Off	4-2
SP	Sweep Stop Frequency	4-2
SQS	SRQ After a Number of Sweeps	4-3
SSM	Sweep Standard Mode	4-2
ST	Sweep Start Frequency	4-2
SW	Sweep Width	4-2
	T	
TMO	Print Tabulation, Markers Only	4-2
TST	Self Test	4-2
T02	Print Tabulation 26 Frequencies	4-2
T05	Print Tabulation 51 Frequencies	4-2
T10	Print Tabulation, 101 Frequencies	4-2
T20	Print Tabulation, 201 Frequencies	4-2
T40	Print Tabulation, 401 Frequencies	4-2

SECTION V
PERFORMANCE VERIFICATION

SECTION V
PERFORMANCE VERIFICATION

5-1 INTRODUCTION

This section provides performance verification procedures for the Model 6407/-6409 RF Analyzer. All performance tests are verfied from the RF Analyzer control panel. No internal circuits or controls are disturbed. If all tests are within the specified tolerances, the RF Analyzer requires no calibration, and no calibration should be attempted.

5-2 RECOMMENDED TEST EQUIPMENT

Table 5-1 provides a list of the recommended test equipment for performance verification. However, if recommended test equipment items are not available, equipment with equivalent characteristics may be substituted.

5-3 TEST RECORDS

Tables 5-2, 5-3, 5-5, and 5-6 are forms that can be photocopied and used to keep an accurate performance verification test record. These tables are found in the applicable sections of the performance verification procedure.

5-4 CW FREQUENCY ACCURACY TEST

The CW Frequency Accuracy Test verifies that the CW accuracy of the 6407 or 6409 is within 100 kHz.

a. Equipment Required.

EIP 545A Counter, or equivalent.

b. Procedure.

1. Before connecting the test equipment as shown in Figure 5-1, turn the equipment on.

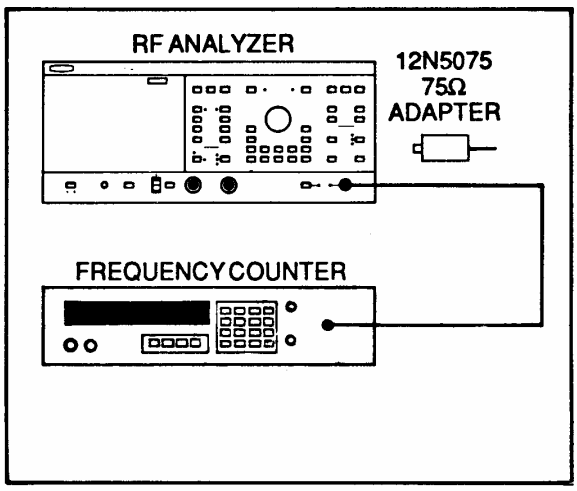


Figure 5-1. Test Setup for CW Frequency Accuracy Test

2. On the RF Analyzer,
   (a) Press RESET, SELECT.
   (b) Press the POWER LEVEL key and set for +5 dBm.
3. Connect the frequency meter to the RF Analyzer.
4. On the counter:
   (a) Connect the RF test cable to BAND 1 for the 6407, or to BAND 2 for the 6409.
   (b) Press BAND then either "1" or "2" as appropriate.
   (c) Press RESOL then "3" to set for 100 kHz resolution.
5. On the RF Analyzer,
   (a) Press the NETWORK ANALYZER, CHANNEL A and CHANNEL B ON/OFF keys to OFF.

Table 5-1. Recommended Test Equipment for Performance Verification and Calibration of the 6407/6409 RF Analyzer.

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED MANUFACTURER
Digital Multimeter	DC Volts: 3-1/2 digit resolution	John Fluke, Inc. Model 8840A
Oscilloscope	60 MHz bandwidth. 1mV sensitivity.	Tektronix 3313A or Philips Model PM 3267
Frequency Counter	10 MHz to 7 GHz range.	EIP Model 545A or HP 5350A
RF Power Meter	1 MHz to 7 GHz range. +13 to -60 dBm measurement capability. 50/75Ω.	HP 436A + HP8482A or HP8484A, 50Ω heads, or HP8483A, 75Ω head.
Spectrum Analyzer	60 dB power range. 10 MHz to 7 GHz range. 50 dB signal-to-noise ratio, .01 to 2 GHz.	HP 8565A or Tektronix 492
Modulation Meter	15 kHz bandwidth.	Racal 9008A or Marconi TF2304
Adjustable AC Line Transformer (Variac)	100/120V line voltage. 220/240V line voltage.	General Radio W5MTB, General Radio W10HM73
Line Voltage Monitor	120V line voltage. 240V line voltage.	RCA 120B RCA WV 503A
Peak Filter	500 MHz Saw Filter	T858, WILTRON
Low Pass Filter	150 MHz, 7 Section LPF	K&L Microwave,Inc. Model 7L120-150- N/NP
T856 Extender Connector		WILTRON

(b) Press the SOURCE, FREQUENCY WIDTH key; enter 0 MHz when the menu appears.

(c) Press the FREQUENCY CENTER key and enter 1 MHz (6407) or 10 MHz (6409).

(d) Press the DATA ENTRY, ENTER key a second time.

NOTE

When a frequency is entered, it is frequency locked to the reference then released. After release, the frequency may drift. Pressing ENTER a second time reinstitutes a frequency lock. During normal operation--i.e., if either or both channels are open--the frequency automatically locks at the start of every sweep, even when the sweep width is zero.

6. Verify that the frequency displayed on the counter is within 100 kHz of the requested RF Analyzer frequency.

7. For the 6407, move the RF test cable to the BAND 2 input on the counter.

8. Using the RF Analyzer DATA ENTRY keypad, enter 100 MHz for either the 6407 or 6409.

9. Verify that the frequency displayed on the counter is within 100 kHz of the requested RF Analyzer frequency.

10. Repeat steps 8 and 9 at 100 MHz increments, up to 1000 MHz for the 6407 or 2000 MHz for the 6409.

11. Record the counter readings on the chart in Table 5-2.

5-5 OUTPUT POWER FLATNESS TEST

The Output Power Flatness Test verifies that the output power from the RF source in the 6407 or 6409 is within specified limits. These limits are:

50Ω Output, no built-in attenuator:
±0.3 dB

50Ω Output, with built-in attenuator:
±1 dB ±0.1 dB/10 dB step

75Ω Output, no built-in attenuator:
±0.5 dB

75Ω Output, with built-in attenuator:
±1 dB ± 0.1 dB/10 dB step

A chart that you can copy, and one that will aid you in recording the tested power levels, is contained in Table 5-3.

a. Equipment Required.

Hewlett-Packard 436A Power Meter

b. Procedure.

1. Calibrate the power meter/power sensor to obtain an accurate power reading. Refer to the applicable procedure in the HP436A Operating and Service Manual.

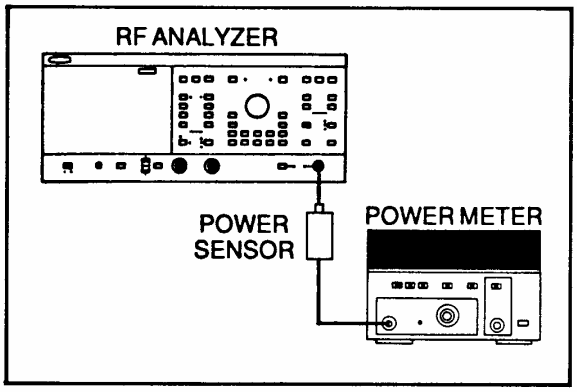


Figure 5-2. Test Setup for Output Power Flatness Test

Table 5-2. Frequency Accuracy Chart

FREQUENCY ACCURACY CHART		
CW FREQUENCY(MHz)	COUNTER READING (MHz)	SPECIFICATION RANGE (MHz)
1		0.99 to 1.1
10		9.9 to 10.1
100		99.9 to 100.1
200		199.9 to 200.1
300		299.9 to 300.1
400		299.9 to 400.1
500		499.9 to 500.1
600		599.9 to 600.1
700		699.9 to 700.1
800		799.9 to 800.1
900		899.9 to 900.1
1000		999.9 to 1000.1
1100		1099.9 to 1100.1
1200		1199.9 to 1200.1
1300		1299.9 to 1300.1
1400		1399.9 to 1400.1
1500		1499.9 to 1500.1
1600		1599.9 to 1600.1
1700		1699.9 to 1700.1
1800		1799.9 to 1800.1
1900		1899.9 to 1900.1
2000		1999.9 to 2000.1

Table 5-3. Output-Power Flatness Test Chart

OUTPUT-POWER FLATNESS TEST

Frequency/Power Chart

Frequency_____

50 Ohm Output, Without Attenuator

SETTING (dBm)	READING (dBm)	SPECIFICATION RANGE (dBm)
+12	_____	+11.7 to +12.3
+2	_____	+1.7 to +2.3

50 Ohm Output, With Attenuator

SETTING (dBm)	READING (dBm)	SPECIFICATION RANGE (dBm)
+10	_____	+9 to +11
0	_____	-1.1 to +1.1
-10	_____	-11.2 to -8.8
-20	_____	-21.3 to -18.7
-30	_____	-31.4 to -28.6
-40	_____	-41.5 to -38.5
-50	_____	-51.6 to 48.4

75 Ohm Output, Without Attenuator

SETTING (dBm)	READING (dBm)	SPECIFICATION RANGE (dBm)
+10	_____	+9.5 to +10.5
+0	_____	-0.5 to +0.5

75 Ohm Output, With Attenuator

SETTING (dBm)	READING (dBm)	SPECIFICATION RANGE (dBm)
+8	_____	+7.5 to +8.5
-2	_____	-3.1 to -0.9
-12	_____	-13.1 to -10.9
-22	_____	-23.3 to -20.7
-32	_____	-33.4 to -30.6
-42	_____	-43.5 to -40.5
-52	_____	-53.6 to 50.4

Note: Below -50 or -52 dBm the leveled power cannot be checked except over the GPIB. At those low power levels, the readings have to be averaged over time.

2. Setup test equipment per Figure 5-2, and turn the equipment on.

3. On the RF Analyzer,

   (a) Press the SYSTEM FUNCTIONS, RESET key, then the NETWORK ANALYZER, MENU SELECT key to return to the default settings.

   (b) Press the NETWORK ANALYZER, CHANNEL A and CHANNEL B ON/OFF keys to OFF.

   (c) Press the SOURCE, FREQUENCY WIDTH key; enter 0 MHz when the menu appears.

   (d) Press the FREQUENCY CENTER key and enter 1 MHz (6407) or 10 MHz (6409).

4. Verify that the power meter reads the levels shown in Table 5-3.

5. On the RF Analyzer, enter 100 MHz for either the 6407 or 6409.

6. Verify that the power meter reads the levels shown in Table 5-3.

NOTE

Measurements at RF and microwave frequencies can have inaccuracies of up to 50%, due to the inherent inaccuracies of the test equipment and test-connection power matches. Refer to the discussion titled "Power Measurement Accuracy," in the 436A Operating and Service Manual.

7. Repeat steps 5 and 6 at increments of 100 MHz up to 1000 MHz for the 6407, or up to 2000 MHz for the 6409. Return the frequency setting to 1 MHz (6407) or 10 MHz (6409).

8. On the RF Analyzer, press the POWER LEVEL key and decrease the level by 10 dB.

9. Verify that the power meter reads the levels shown in Table 5-3.

10. Repeat steps 7 thru 9.

5-6 SIGNAL PATH ACCURACY TEST

This test verifies the power accuracy of the network analyzer A and B signal paths. The accuracy of these paths is determined by the signal channel's log-amplifier accuracy and the RF detector's frequency-response accuracy.

Both of these accuracy terms are vectors that algebraically add to produce a combined term. In a worst-case situation, both terms could add at their maximum-plus or maximum-minus error value. However, adding in this manner is unlikely. Therefore, the accepted method of determining the uncertainty these two terms provide is a root-sum-square (RSS) calculation--that is:

$$\sqrt{(\text{Ch. Accuracy})^2 + (\text{Det. Freq. Response})^2}$$

Table 5-4 shows these accuracy terms. The procedure for making an accuracy measurement is shown below.

a. Equipment Required.

   Hewlett-Packard 436A Power Meter

b. Procedure.

   1. Calibrate the power meter/power sensor to obtain an accurate power reading. Refer to the

Table 5-4. Signal Channel Path Specifications

OUTPUT POWER (dBm)	CHANNEL ACCURACY (dB)	DETECTOR FREQ. RESPONSE @50 MHz (dB)	RSS SIGNAL PATH ACCURACY (dB)
+16	0.5	0.2	0.54
+10	0.35	0.2	0.4
+5	0.32	0.2	0.38
0	0.3	0.2	0.36
-5	0.35	0.2	0.4
-10	0.4	0.2	0.45
-15	0.45	0.2	0.49
-20	0.55	0.2	0.59
-25	0.60	0.2	0.63
-30	0.65	0.2	0.68
-35	0.73	0.2	0.76
-40	0.8	0.2	0.82
-45	1.0	0.2	1.02
-50	1.2	0.2	1.22
-55	2.0	0.2	2.01

applicable procedure in the HP436A Operating and Service Manual.

2. Setup test equipment as shown in Figure 5-3, and turn the equipment on.

3. Frequency Source Calibration, Without Attenuator Option Fitted

   (a) Set the step attenuator for 0 dB.

   (b) On the RF Analyzer,

      (1) Press the SYSTEM FUNCTIONS, RESET key, then the NETWORK ANALYZER, MENU SELECT key to return to the default settings.

      (2) Press the NETWORK ANALYZER, CHANNEL A and CHANNEL B ON/OFF keys to OFF.

      (3) Press the SOURCE, FREQUENCY, WIDTH key; enter 0 MHz when the menu appears.

      (4) Press the FREQUENCY CENTER key and enter 50 MHz.

   (c) Copy the chart in Table 5-5, then record the power meter reading in the appropriate space.

   (d) On the RF Analyzer, press the POWER LEVEL key and enter +5 dBm.

   (e) Record the power meter reading in the appropriate space on your copy of the chart from Table 5-5.

   (f) On the analyzer, enter +10 dBm.

   (g) Decrease the step attenuator by 10 dB.

   (h) Record the power meter reading.

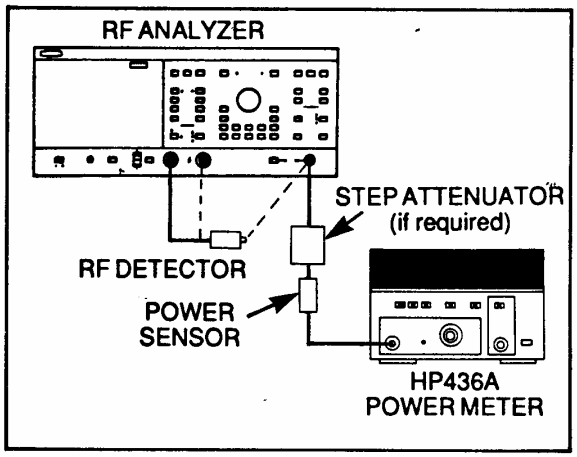


Figure 5-3. Test Setup for Signal Path Accuracy

Table 5-5. Signal Channel Accuracy Chart, Without Attenuator

SIGNAL CHANNEL ACCURACY CHART, WITHOUT ATTENUATOR				
ATTENUATOR SETTING	POWER METER READING (dBm)	SIGNAL CHANNEL READING (dBm)	SIGNAL CHANNEL ACCURACY (dBm)	SPECIFICATION ACCURACY (dB)
0				0.4
5				0.44
10				0.36
15				0.4
20				0.45
25		[1]		0.49
30				0.54
35	[2]			0.58
40		[3]		0.63
45				0.68
50				0.73
55				0.87
60				1.0
65				1.2

[1] Set SMOOTHING to light the MIN indicator.
[2] Change to the HP8484A Power Sensor.
[3] Set SMOOTHING to light the MAX indicator.

(i) Repeat steps d. and e. for the chart's remaining attenuator settings.

4. Channel Accuracy Verification, Without the Attenuator Option Fitted

(a) Disconnect the power sensor from the step attenuator output.

(b) Connect the RF detector to the step attenuator output.

(c) Press the NETWORK ANALYZER, CHANNEL A DISPLAY ON/OFF key to ON.

(d) Press the NETWORK ANALYZER, MENU key.

(e) Ensure that the SET MEASUREMENT TYPE option is highlighted on the menu display, then press SELECT.

(f) When the next menu appears, move the menu cursor to highlight the POWER dBm option, then press SELECT.

(g) Set the step attenuator for 0 dB.

(h) Press the POWER LEVEL key and set for +10 dBm.

(i) Press the SOURCE, MARKERS key.

(j) Select the M1 marker when the menu appears. (Ensure that the M1 marker is highlighted.)

(k) On the DATA ENTRY keypad, press 50, then press ENTER to set the M1 value for 50 MHz.

(l) Read the M1 value from the READOUT menu, then record it in the chart.

(m) Press the POWER LEVEL key and set for +5 dBm.

(n) Read the M1 value from the READOUT menu, then record it in the chart.

(o) On the step attenuator, increase the attenuation by 10 dB.

(p) Set source power for +10 dBm.

(q) Read the M1 value from the READOUT menu, then record it in the chart.

(r) Repeat steps l. thru p. for the chart's other attenuator settings.

(s) In the chart, subtract the values in the "Signal Channel Reading" column from those in the "Power Meter Reading" column; enter the difference value in "Signal Channel Uncertainty" column.

(t) Verify that the uncertainty values are within the specification accuracy.

(u) Move the detector input from Channel A to Channel B.

(v) Press the CHANNEL A DISPLAY ON/OFF key to OFF and the CHANNEL B DISPLAY ON/OFF key to ON.

(w) Repeat steps 3.d thru 3.t above.

5. Frequency Source Calibration, With Attenuator Option Fitted

(a) Calibrate the power meter/-power sensor to obtain an accurate power reading. Refer to the applicable procedure in the HP436A Operating and Service Manual.

(b) Connect the power meter as shown in Figure 5-3.

(c) On the RF Analyzer,

(1) Press the SYSTEM FUNCTIONS, RESET key, then the NETWORK ANALYZER, MENU SELECT key to return to the default settings.

(2) Press the NETWORK ANALYZER, CHANNEL A and CHANNEL B ON/OFF keys to OFF.

(3) Press the SOURCE, FREQUENCY WIDTH key; enter 0 MHz when the menu appears.

(4) Press the FREQUENCY CENTER key and enter 50 MHz.

(d) Copy the chart in Table 5-6, then record the power meter reading in the appropriate space.

(e) On the RF Analyzer, press the POWER LEVEL key and enter +5 dBm.

(f) Record the power meter reading in the appropriate space on your copy of the chart from Table 5-6.

(g) Decrease the analyzer power by 5 dB.

(h) Record the power meter reading.

(i) Repeat steps g. and h. for the chart's remaining source-power settings.

6. Channel Accuracy Verification, With the Attenuator Option Fitted

(a) Disconnect the power sensor from the RF OUTPUT connector.

(b) Connect the RF detector from Channel A to the RF OUTPUT connector.

(c) Press the NETWORK ANALYZER, CHANNEL A DISPLAY ON/OFF key to ON.

(d) Press the NETWORK ANALYZER, MENU key.

(e) Select the SET MEASUREMENT TYPE option when the menu appears.

(f) Select the POWER dBm option when the next menu appears.

(g) Press the POWER LEVEL key and set for +10 dBm.

(h) Press the SOURCE MARKERS key.

(i) Select the M1 marker when the menu appears.

(j) Set the M1 value for 50 MHz.

(k) Read the M1 value from the READOUT menu, then record it in the chart.

(l) Press the POWER LEVEL key and set for +5 dBm.

Table 5-6. Signal Channel Accuracy Chart, With Attenuator

SIGNAL CHANNEL ACCURACY CHART				
SOURCE POWER LEVEL (dBm)	POWER METER READING (dBm)	SIGNAL CHANNEL READING (dBm)	SIGNAL CHANNEL ACCURACY (dBm)	SPECIFICATION ACCURACY (dB)
+16[1]				0.45
+10(+8)[2]				0.4
+5				0.44
0				0.36
-5				0.4
-10				0.45
-15				0.49
-20				0.54
-25	[3]	[4]		0.58
-30				0.63
-35				0.68
-40		[5]		0.73
-45				0.87
-50				1.0
-55				1.2

[1] An external amplifier has to be used to obtain +16 dBm from the source. See paragraph 5-6.5.
[2] +8 dBm is the maximum power available from the 6407 having an attenuator option fitted.
[3] Change to the HP8484A Power Sensor.
[4] Set SMOOTHING to light the MIN indicator.
[5] Set SMOOTHING to light the MAX indicator.

(m) Read the M1 value from the READOUT menu, then record it in the chart.

(n) Decrease the power by 5 dB.

(o) Read the M1 value from the READOUT menu, then record it in the chart.

(p) Repeat steps 1. thru o. for the chart's other source-power settings.

(q) In the chart, subtract the values in the "Signal Channel Reading" column from those in the "Power Meter Reading" column; enter the difference value in "Signal Channel Uncertainty" column.

(r) Verify that the uncertainty values are within the specification range.

(s) Move the detector input from Channel A to Channel B.

(t) Press the CHANNEL A DISPLAY ON/OFF key to OFF and the CHANNEL B DISPLAY ON/OFF key to ON.

(u) Repeat steps 5.d thru 5.r above.

5-7 RESIDUAL FM TEST

This test verifies that the residual FM from the frequency source is ≤5 kHz. This test assumes use of the Marconi TF2304 Modulation Meter, which goes to 1000 MHz. To test frequencies above 1 GHz, you can down convert the frequencies using the TEK 492 Spectrum Analyzer.

a. Equipment Required.

Marconi TF2304 Modulation Meter and Tektronix 492 Spectrum Analyzer.

b. Procedure.

1. Setup the test equipment as shown in Figure 5-4, and turn the equipment on.

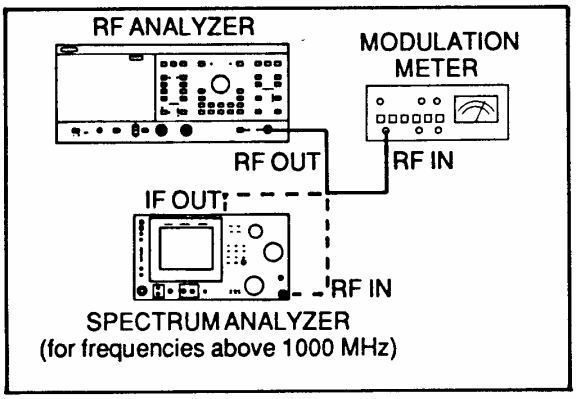


Figure 5-4. Test Setup for Residual FM Test

2. On the RF Analyzer,

(a) Press the POWER LEVEL key and set for +5 dBm.

(b) Press the NETWORK ANALYZER, CHANNEL A and CHANNEL B ON/OFF keys to OFF.

(c) Press the SOURCE, FREQUENCY WIDTH key; enter 0 MHz when the menu appears.

(d) Press the FREQUENCY CENTER key and enter 500 MHz (6407) or 1000 MHz (6409).

3. On the modulation meter, after ensuring the HIGH and LOW

indicators are not lit, read the frequency deviation meter. Ensure that the meter reads ≤5 kHz.

4. For the 6409, to test frequencies above 1000 MHz proceed as follows:

   (a) On the spectrum analyzer:

   (1) Adjust TUNING to center the source output frequency on the CENTER FREQUENCY graticule line.

   (2) Adjust the REFERENCE LEVEL control to place the top of the waveform on the REFERENCE LEVEL graticle line.

   (3) Set FREQUENCY SPAN/DIV to 20 MHz.

   (4) Observe the display; it should resemble that shown in Figure 5-6.

   (5) Set FREQUENCY SPAN/DIV to 10 ms (zero span) and readjust TUNING to place the trace on the REFERENCE LEVEL graticule line.

   (6) If applicable, position AUTO STABILIZER to ON; if necessary, readjust the TUNING control to place the trace on the REFERENCE LEVEL graticule line.

   (b) On the modulation meter, after ensuring the HIGH and LOW indicators are not lit, read the frequency deviation meter. Ensure that the meter reads ≤5 kHz.

5-8 SOURCE OUTPUT SIGNAL TEST

This test verifies that the close-in sidebands are <-40 dBc and that the harmonic and non-harmonic (spurious) signals from the frequency source are <-30 dBc (except -25 dBc on the 6407 between 1 and 2 MHz) and <-40 dBc, respectively.

a. Equipment Required.

Tektronics 492 Spectrum Analyzer, or equivalent. An equivalent analyzer will need a frequency range of 1 to 1000 MHz, for the 6407, or 10 to 2000 MHz, for the 6409.

b. Procedure for checking close-in sidebands.

1. Setup the test equipment as shown in Figure 5-5, and turn the equipment on.

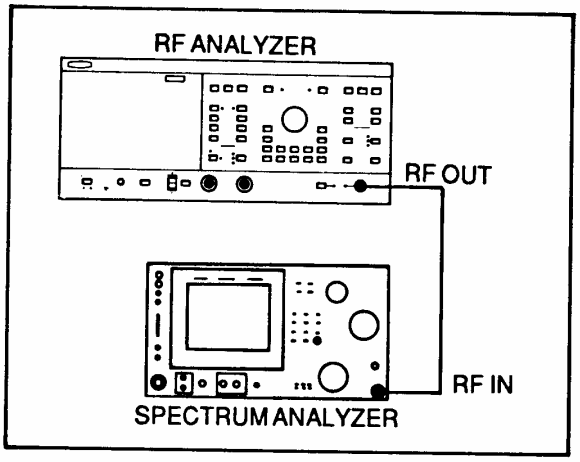


Figure 5-5. Test Setup for Output Signal Test

2. On the 6400 RF Analyzer,

   (a) Press the POWER LEVEL key and set for +5 dBm.

   (b) Press the NETWORK ANALYZER, CHANNEL A and CHANNEL B ON/OFF keys to OFF.

(c) Press the SOURCE, FREQUENCY WIDTH key; enter 0 MHz when the menu appears.

(d) Press the FREQUENCY CENTER key and enter 500 MHz (6407) or 1000 MHz (6409).

3. On the 492 spectrum analyzer:

(a) Adjust the FREQUENCY and FREQUENCY RANGE controls to view the 6400 output signal.

(b) Adjust the MIN RF ATTEN control for 30 dB.

(c) Adjust the REFERENCE LEVEL control for 0 db/division.

(d) Adjust the FREQUENCY SPAN/DIV and RESOLUTION BANDWIDTH controls to display the two sidebands of the 6400 output-signal (Figure 5-6).

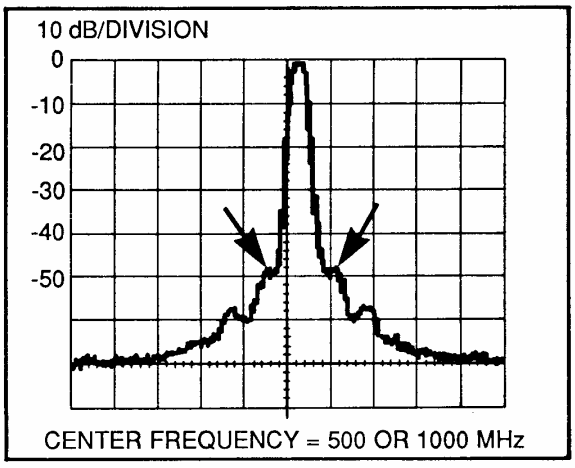


Figure 5-6. 6400 Output Signal and Close-in Sidebands

These sidebands are located approximately 16 kHz (50 Hz line frequency) or 19.2 kHz (60 Hz line frequency) away from the output signal, and should be <-40 dBc.

c. Procedure for checking harmonic and non-harmonic signals.

1. Set up the test equipment as described in paragraph 5-8.b, steps 1 thru 3.

2. Starting at the low end of the frequency range, increase the 6400 output signal toward the high end of the band and observe that the harmonics remain within their specified tolerances, as follows:

(a) On the 6400, use the rotary knob to increase the 6400 signal toward its high-end frequency.

(b) On the spectrum analyzer, adjust the FREQUENCY tuning control, FREQUENCY SPAN/DIV and RESOLUTION BANDWIDTH controls to track the 2nd and 3rd harmonics as they move across the screen.

3. Verify that the 2nd harmonic does not exceed -30 dBc.

4. Return the 6400 frequency to the low end of the band.

5. Repeat step 4 to check for non-harmonically related (spurious) signals.

NOTE

Spurious signals may be generally characterized as follows: They will be low in amplitude, they will appear and disappear abruptly, and they will track opposite to the fundamental and harmonic signals.

6. Verify that any spurious signals are <-40 dBc.

SECTION VI
CALIBRATION

SECTION VI
CALIBRATION

6-1 INTRODUCTION

This section contains 6407/6409 RF Analyzer calibration procedures, which are organized as follows:

Para.	Calibration
6-4	A4 Sweeper PCB
6-5	A3 Signal Channel PCB
6-6	CRT Set Up

Access to the instrument interior is gained by removing the four corner brackets and sliding the covers off (Figure 6-1).

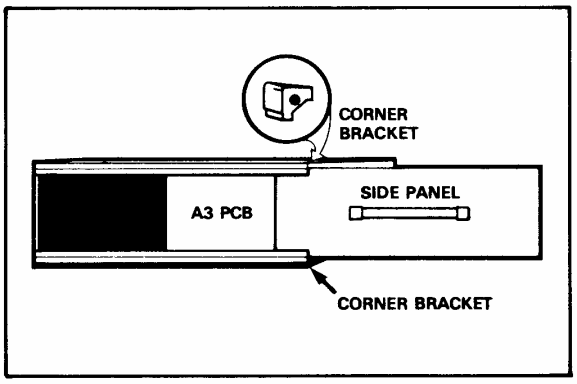


Figure 6-1. Gaining Access to RF Analyzer PCBs

6-2 RECOMMENDED TEST EQUIPMENT

The test equipment recommended for calibration of the 6407/6409 RF Analyzer is listed in Table 5-1.

6-3 ADJUSTMENTS FOLLOWING PCB REPLACEMENT.

Table 6-1 lists the required calibration following the replacement of PCBs.

6-4 A4 SWEEPER PCB ADJUSTMENTS

The A4 sweeper PCB is located on the bottom of the RF Analyzer beneath the RF deck. To make adjustments on this board, remove the bottom cover. Set the unit on its side so that you can access the adjusting pots on the board while also entering parameters from the control panel.

NOTE

The 6400 RF Analyzer cooling system is designed to operate with the covers on. If you are working in a warm environment with the covers off, it is possible that the current-limiting polyswitches on the power supply board (A9) could

Table 6-1. Recommended Adjustments Following PCB Replacement

If the Following PCB Was Replaced:	Perform the Following Adjustments in Section(s):
A3 PCB	6-5.1, 6-5.2
A4 PCB	6-4.1, 6-4.2, 6-4.3, 6-4.4

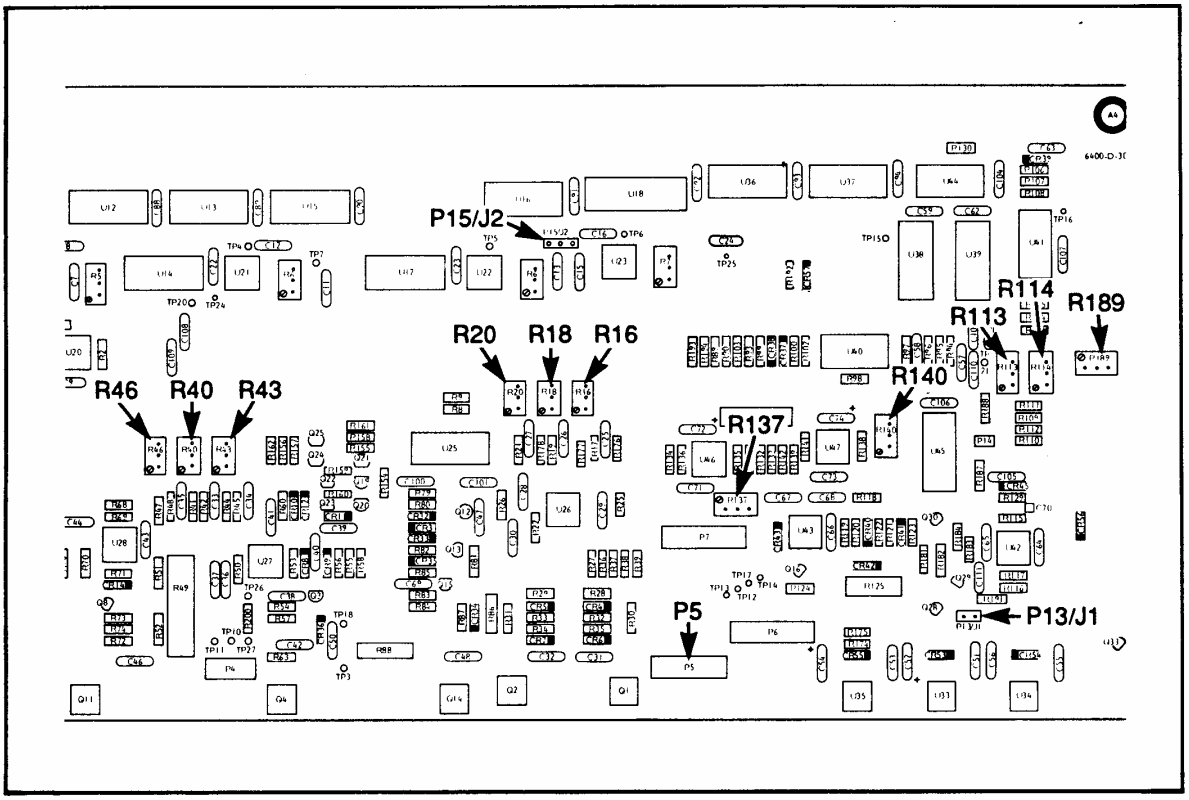


Figure 6-2. Locations of A4 PCB Adjustments

trip, which would limit power to the circuits. This is not an instrument failure, but merely a protective action built into the instrument. If this occurs, turn the instrument OFF and allow it to cool before proceeding with the calibration.

The A4 PCB adjustment pots referenced in the text are called out in Figure 6-2.

6-4.1 Main Tuning Coil Calibration

1. With the RF Analyzer power OFF, insert the T856 extender connector between P5 and the YIG cable that plugs into P5 as shown in Figure 6-3.

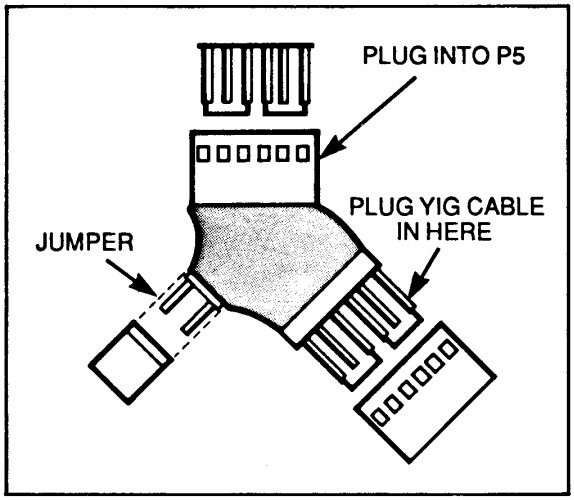


Figure 6-3. T856 Extender Connector

6-4.1 Main Tuning Coil Calibration

3. With the RF Analyzer power OFF, insert the T856 extender connector between P5 and the YIG cable that plugs into P5 as shown in Figure 6-3.

4. Switch the RF Analyzer ON and allow for a 30 minute warm-up period.

5. On the RF Analyzer control panel:
   (a) Press RESET then SELECT.
   (b) Ensure that Channels A and B are OFF.
   (c) Press the SOURCE FREQUENCY, WIDTH and enter 0 MHz.
   (d) Press the SOURCE FREQUENCY, CENTER key and enter 10 MHz.
   (e) Enter a power level of 0.1 dBm.

6. Cycle the YIG by:
   (a) Setting the center frequency to 1000 MHz.
   (b) Then setting the center frequency to 10 MHz.
   (c) Repeat steps 4a and 4b three or four times.

7. Remove the jumper from the T856 extender connector as shown in Figure 6-3.

8. Connect the frequency counter to the output of the RF Analyzer as shown in Figure 6-4.

9. On the RF Analyzer, set the center frequency to 10 MHz, then to 50 MHz. Allow for a settle time of 10 seconds.

10. On the A4 board, adjust R46 until the frequency counter reads 50 MHz ±500 kHz. Always adjust the frequency from low to high. If you overshoot this value, readjust R46 for a value less than 50 MHz and repeat the step.

11. Does a clockwise adjustment increases frequency? If it does not, turn R46 clockwise until 50 MHz is found.

    This may only be necessary once. It is caused by moving below 0 MHz to -50 MHz.

12. On the RF Analyzer control panel, set the center frequency to 2000 MHz (6409) or 1000 MHz (6407). Allow a 10 second settling time.

13. On the A4 board, adjust R40 until the frequency counter reads as set above (2000 or 1000 MHz) ±500 kHz.

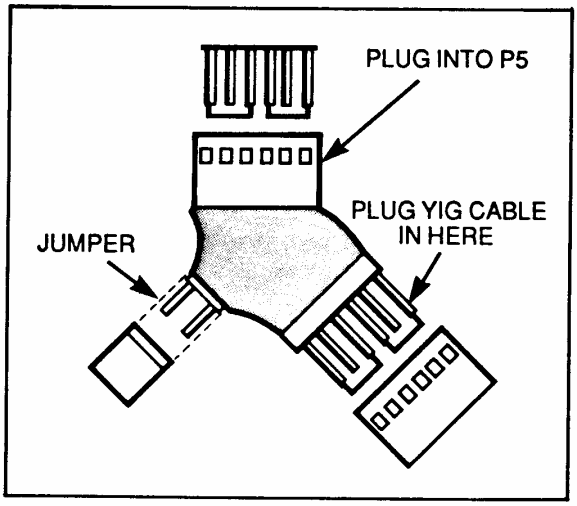


Figure 6-3. T856 Extender Connector

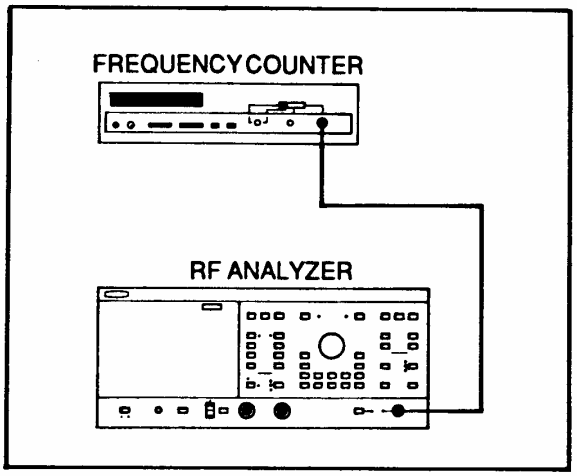


Figure 6-4. Main Tuning Coil Calibration Test Setup

14. Repeat steps 7 thru 11 until no further adjustments are necessary.

15. On the RF Analyzer control panel, set the center frequency to 10 MHz, then to 1000 MHz (6409) or 500 MHz (6407).

16. Record the frequency counter reading. Frequency = _____ MHz.

17. Calculate the difference, or error, between the set and measured frequencies, then divide by two.

    For example, if the set frequency was 1000 MHz and the measured frequency was 999.6, then the difference would be 0.4 MHz; divided by 2, the quotient = 0.2 MHz. Record the calculated value: _____ MHz.

18. On the RF Analyzer, set the center frequency to 10 MHz, then to 50 MHz. Allow a ten second settling time.

19. If the reading on the frequency counter is greater than the value set, adjust A4R46 to reduce the counter by the value (in MHz) recorded in step 15.

20. If the reading on the frequency counter is less than the value set, adjust A4R46 to increase the frequency counter by the value (in MHz) recorded in step 15.

21. On the RF Analyzer control panel, set Start to 100 MHz and set Stop to 150 MHz.

22. Record the counter reading: _____ MHz (it should be 100 MHz ±4 MHz).

23. On the RF Analyzer control panel, set Stop to 2000 MHz (6409) or 1000 MHz (6407).

24. On the A4 board, adjust R43 until the frequency counter reads the value recorded in step 20 to within 200 kHz.

25. Repeat steps 19 thru 22 as necessary until the adjustment is stable.

6-4.2 FM Coil Calibration

a. Centering

1. Set up the test equipment as shown in Figure 6-5.

2. On the A4 board, replace the jumper on the T856 extender connector.

3. On the RF Analyzer control panel:
   (a) set the frequency Width to 50 MHz.
   (b) set Center frequency to 1000 MHz (6409) or to 500 MHz (6407).

4. On the A4 board:
   (a) Remove the jumper on P15 (J2) from pins 2 and 3.

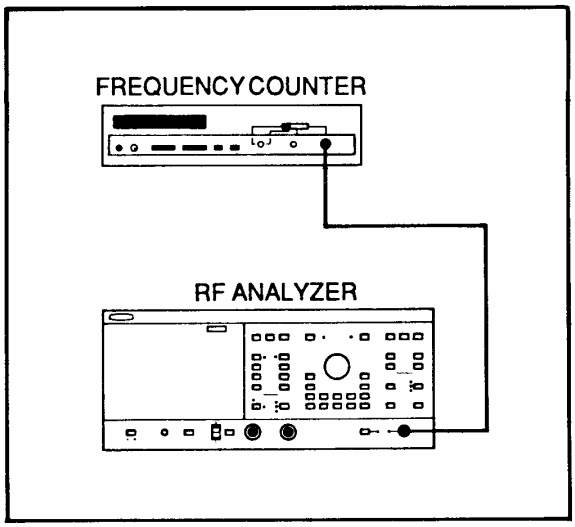


Figure 6-5. FM Coil Calibration Test Setup

6-4.4 ALC Power Calibration

a. Pre-calibration of A4 PCB

1. Adjust A4R118 fully clockwise. On the 6407, turn A4R118 counter-clockwise to the six o'clock position. On the 6409, turn A4R118 counter-clockwise to the four o'clock position. Refer to Figure 8-59 for the correct configuration of A4P16.

2. Switch the 6400 on and press RESET. Connect a known good detector to Input A and the RF output and set Channel A to read POWER.

3. Set up a marker at the mid-frequency of the 6400 and adjust A4R140 to read the reset power ±0.2 dB.

4. Set the source power to +0.1 dBm and adjust A4R137 to read 0.1 ±0.2 dBm.

5. Set the source power to 0.1 dBm and press AUTOSCALE. Adjust A4R113 for the best slope.

NOTE

Jumper A4J3 may be positioned in either "a" or "b" depending on the direction of slope compensation required. A4J3 may not be fitted to some older boards.

NOTE

When making the final adjustment of A4R118, adjust A4R118 counter-clockwise until the UNLEVELED light begins to flash. Then turn slightly clockwise until the UNLEVELED light stops flashing.

b. Calibration Below 10 dBm.

1. On the power meter:
   (a) Zero and calibrate the power meter.
   (b) Ensure that the correct impedance is used (50 or 75 Ohm).
   (c) Ensure that the correct CAL FACTOR is set for 1000 MHz (6409) or 500 MHz (6407).

2. Turn the RF Analyzer ON, and
   (a) Set Start to 10 MHz (6409) or 1 MHz (6407).
   (b) Set Stop to 2000 MHz (6409) or 1000 MHz (6407).
   (c) Connect a known-good detector from channel A to the output of the RF Analyzer.
   (e) Switch channel A to ON.
   (f) Switch channel B to OFF.
   (g) Set power level to 1 dBm.
   (h) Press the Channel A Menu key and ensure that the menu cursor highlights SET MEASUREMENT TYPE.
   (i) Press SELECT.
   (j) Move the menu cursor to highlight POWER dBm, then press SELECT.
   (k) Press AUTOSCALE.

3. On the A4 board, adjust R113 for the best slope across the band. The trace across the display should be relatively flat.
   The specification is as follows:
   ±1.0 dB - 70 dB attenuator fitted.
   ±0.50 dB - no attenuator, 75Ω.
   ±0.30 dB - no attenuator, 50Ω

4. On the RF Analyzer, set a CW frequency of 1000 MHz (6409) or 500 MHz (6407).

5. Disconnect the detector from the RF Analyzer output.

6. On the RF Analyzer, switch Channel A OFF.

7. Connect the power meter to the output of the RF Analyzer as shown in Figure 6-7.

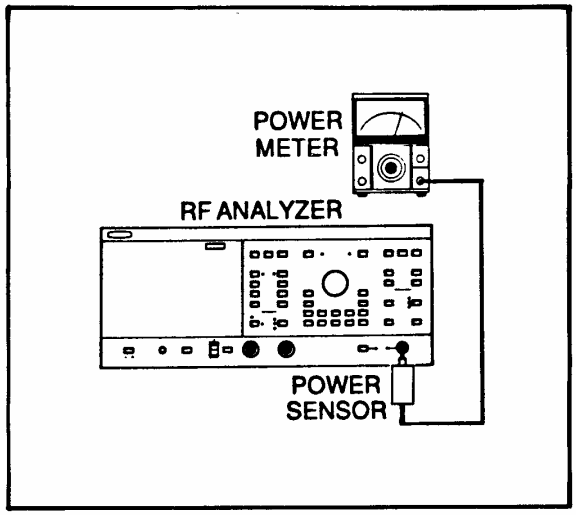


Figure 6-7. ALC Power Calibration Test Setup

8. Set the RF Analyzer power level to 10 dBm. (Set the power level on a 75Ω RF Analyzer with an attenuator to 8 dBm).

9. On the A4 board, adjust R140 until the power meter reads the value set in step 8.

NOTE

A4R135 is a S.O.T resister that may require re-selection folowing a down converter or YIG oscillator replacement.

10. On the RF Analyzer control panel, set the power level to 0.1 dBm.

11. On the A4 board, adjust R137 until the power meter reads +0.1 dbm as set in step 10.

12. Repeat steps 8 thru 11 until the power variation is consistently ±0.03 dB.

13. Verify that adjacent 0.1 dB steps from 0.1 dBm to 1.0 dBm are accurate to within 0.04 dB of each other.

c. <u>Calibration Above 10 dBm.</u>

NOTE

This section is not applicable to 75Ω units with an attenuator (Option 2) fitted.

1. On the RF Analyzer, press RESET then SELECT.

2. Disconnect the power meter from the output of the RF Analyzer.

3. Connect the channel A detector to the output of the RF Analyzer.

4. Turn channel B OFF.

5. Calibrate for transmission by pressing CALIBRATION and following the screen prompts on the RF Analyzer display.

6. When there are no further prompts (blank menu), press AUTOSCALE. A straight line should be observed at 0 dB. (The Channel A trace is at 0 dB. The reference caret is offset +0.4 dB, or 4 divisions above the Channel A trace.)

7. Set the power level to 10.1 dBm.

8. Without adjusting the scaling of the display, adjust A4R114 (slope) and A4R189 (offset) to

obtain a straight line at +0.1 dB (three divisions below reference).

9. Verify that there is a 0.1 dB difference between the lines at power levels of 10.0 and 10.1 dBm.

10. Set a CW frequency of 1000 MHz (6409) or 500 MHz (6407). Ensure that Channels A and B are OFF.

11. Disconnect the detector from the RF Analyzer output.

12. Connect the power meter to the RF Analyzer output.

13. Press POWER LEVEL.

14. Enter power levels of 10.5, 11.0, 11.5, and 12.0 dBm, while verifying the power output.

NOTE

Check your RF Analyzer model's specifications for power output limitations.

15. Disconnect the power meter from the RF Analyzer.

d. Unleveled Operation

1. On the RF Analzyer, press RESET then SELECT.

2. On the A4 board, remove jumper J1 (P13).

3. Verify that the unleveled LED flashes.

4. On the RF Analyzer, press POWER LEVEL.

5. Rotate the analog knob (spinwheel) clockwise to set the power level to maximum. (After the maximum power level is achieved, rotating the spinwheel will no longer have any effect on the power output.)

6. On the A4 board, replace the J1 jumper (P13).

7. Verify that the LED does not light (or flash) while the channel is sweeping.

e. ALC Gain Adjustment

The ALC gain is controlled by A4R118. Adjust R118 as follows:

1. Set the 6407/09 for a full band sweep.

2. Set the output power to maximum (+11 dBm with an attenuator or +13 dBm without the attenuator).

3. Turn R118 fully clockwise (leveled power).

4. Turn R118 counter clockwise until the instrument goes unleveled (LED on control panel lights).

5. Turn R118 back one quarter turn clockwise.

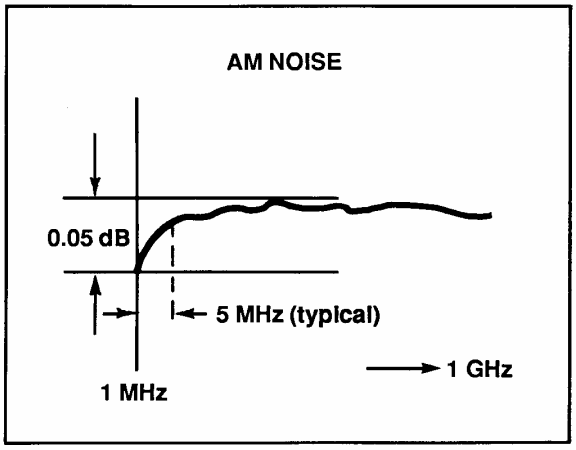
If you are adjusting a 6407 unit, continue with steps 6 thru 10.

6. Measure the AM noise value; it should be <0.05 db.

7. Set the instrument for a full band Transmission measurement.

8. Calibrate the instrument for the transmission measurement; you should get a straight line across the screen.

9. Press AUTOSCALE. The trace should resemble that shown below.



10. If the rise time at the beginning of the trace is out of spec (i.e. the AM noise is >0.05 dB) readjust R118 as necessary to make the correction.

6-5 A3 SIGNAL CHANNEL CALIBRATION

6-5.1 Range Change Error at -20 dBm.

The A3 PCB is located on the right side (as you face the front) of the instrument. The A3 board is exposed when the side panel is removed, as shown in Figure 6-1. Replace the bottom cover if you have not already done so.

The A3 PCB adjustment pots referenced in the text are called out in Figure 6-8.

To perform this calibration, perform the following steps.

1. Connect the test equipment as shown in Figure 6-9.

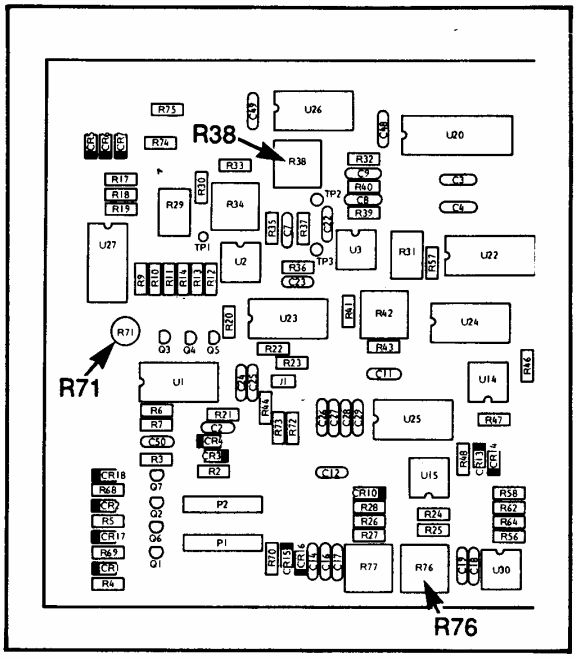


Figure 6-8. Locations of A3 PCB Adjustments

2. On the RF Analyzer:
   (a) Press RESET then SELECT.
   (b) Turn Channel B OFF
   (c) Turn the graticule OFF.
   (d) Press Channel A menu, and ensure that the menu cursor highlighs SET MEASUREMENT TYPE.

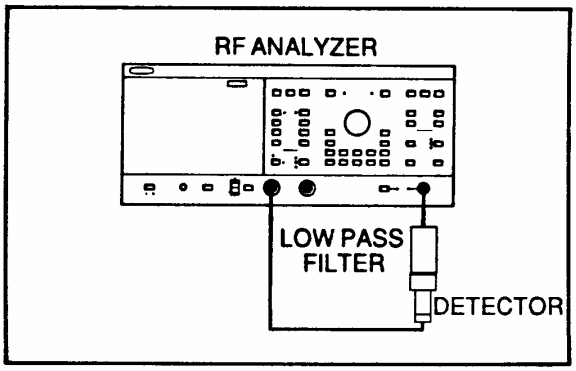


Figure 6-9. Range Change Error Test Setup

(d) Press Channel A menu, and ensure that the menu cursor highlighs SET MEASUREMENT TYPE.
(e) Press SELECT.
(f) Move the menu cursor to highlight POWER dBm, then press SELECT.
(g) Set the Power Level to 0.0 dBm (+0.1 dBm without the optional attenuator).
(h) Press the Channel A menu key and move the menu cursor to highlight SET TEST LIMITS.
(i) Press SELECT, then set Low Limit to -20 dB.
(j) Press the MARKERS key and ensure that the menu cursor highlights M1.
(k) Press ENTER to activate M1.
(l) Using the analog knob (spinwheel), set marker M1 to where the filter skirt intersects the -20 dBm limit line. Note this M1 frequency.

3. On the A3 PCB, adjust R71 fully clockwise.

4. On the RF Analyzer:
   (a) Press SOURCE FREQUENCY, WIDTH and enter 25 MHz.
   (b) Press SOURCE FREQUENCY, CENTER and enter the value noted in step 2.(1).
   (c) Set Resolution to 5.0 dB.
   (d) Press the SOURCE FREQUENCY, CENTER key, then use the analog knob (spinwheel) to position the filter skirt notch at center screen.
   (e) Set Offset to -20 dB.
   (f) Using the analog knob (spinwheel), increase the RESOLUTION to 0.2 dB, while readjusting the OFFSET, as necessary, to keep the filter skirt notch displayed at center screen.

5. Adjust R71 to obtain a smooth trace. The range change should be visible as R71 is adjusted (Figure 6-10).

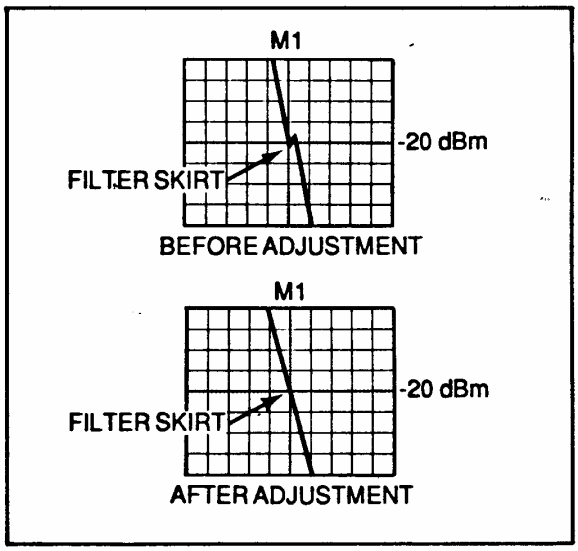


Figure 6-10. R71 Adjustment: Before and After.

6-5.2 Overall Gain Calibration

1. On the power meter:
   (a) Zero and calibrate the power meter.
   (b) Set the correct CAL factor as indicated on the power meter head for 50 MHz.

2. Disconnect the detector from the RF Analyzer, then remove the filter.

3. On the RF Analyzer:
   (a) Press RESET then SELECT.
   (b) Set a CW frequency of 50 MHz.
   (c) Switch Channels A and B OFF.
   (d) Set the power level to 0.1 dBm.
   (e) Set smoothing to MIN.
   (f) Press the Channel A MENU key and ensure that SET MEASUREMENT TYPE is highlighted on the menu display.
   (g) Press SELECT.
   (h) Move the menu cursor to highlight (or select) POWER dBm, then press SELECT.

3. Connect the power meter as shown in Figure 6-11.

NOTE

R76 should need very little adjustment; large adjustments may indicated that another error exists. Ensure that R77 is not adjusted during this setup.

15. Repeat Steps 10 thru 12 until both channels are within 0.02 dB of each other, and within 0.02 of the value set in Step 5.

16. Verify signal channel accuracy by taking readings on channels A and B at 50 MHz using a marker at the desired values for power level.

17. Connect a detector from Channel A to the RF Analyzer output.

18. To ensure electrical stability of the RF Analyzer, replace the side cover.

19. On the RF Analyzer, set
    (a) Smoothing to MAX.
    (b) Power level to -55 dBm.
    (c) OFFSET to -50 dB.
    (d) Resolution to 2 dB/Div.

20. Verify that the overall variation during sweep is contained within 1 division (2 dB).

21. If there is no attenuator option, set the power output level at +5 dBm and use the external step attenuator with 60 dB of attenuation switched in.

NOTE

In order to take readings on the unit, the channel must be ON. When using the power meter, the channels must be OFF.

6-6 CRT SET UP

a. On the RF Analyzer, press RESET then SELECT, then set the display intensity to maximum.

b. On the CRT driver board, located on the left (as you face the front) side of the instrument, adjust the CRT contrast and brightness (brilliance) controls (Figures 6-12) until the display starts to "bloom", or distort, on any of the inverse video blocks. (If there are no inverse video blocks present, open a parameter from the front panel.)

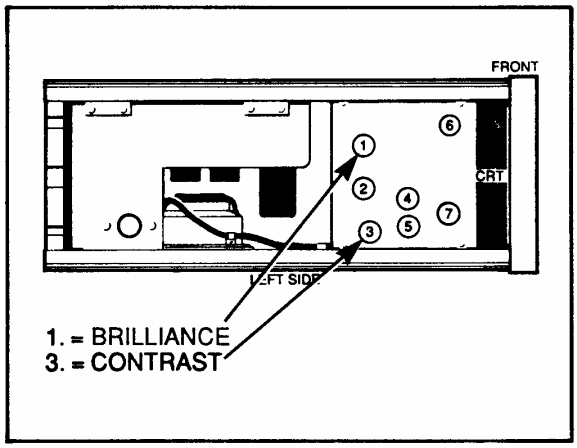


Figure 6-12. CRT Adjustments

c. Using the control panel intensity knob, you should now be able to reduce the screen intensity to a faint display.

NOTE

R76 should need very little adjustment; large adjustments may indicated that another error exists. Ensure that R77 is not adjusted during this setup.

15. Repeat Steps 10 thru 12 until both channels are within 0.02 dB of each other, and within 0.02 of the value set in Step 5.

16. Verify signal channel accuracy by taking readings on channels A and B at 50 MHz using a marker at the desired values for power level.

17. Connect a detector from Channel A to the RF Analyzer output.

18. To ensure electrical stability of the RF Analyzer, replace the side cover.

19. On the RF Analyzer, set
    (a) Smoothing to MAX.
    (b) Power level to -55 dBm.
    (c) OFFSET to -50 dB.
    (d) Resolution to 2 dB/Div.

20. Verify that the overall variation during sweep is contained within 1 division (2 dB).

21. If there is no attenuator option, set the power output level at +5 dBm and use the external step attenuator with 60 dB of attenuation switched in.

NOTE

In order to take readings on the unit, the channel must be ON. When using the power meter, the channels must be OFF.

6-6 CRT SET UP

a. On the RF Analyzer, press RESET then SELECT, then set the display intensity to maximum.

b. On the CRT driver board, located on the left (as you face the front) side of the instrument, adjust the CRT contrast and brightness (brilliance) controls (Figures 6-12) until the display starts to "bloom", or distort, on any of the inverse video blocks. (If there are no inverse video blocks present, open a parameter from the front panel.)

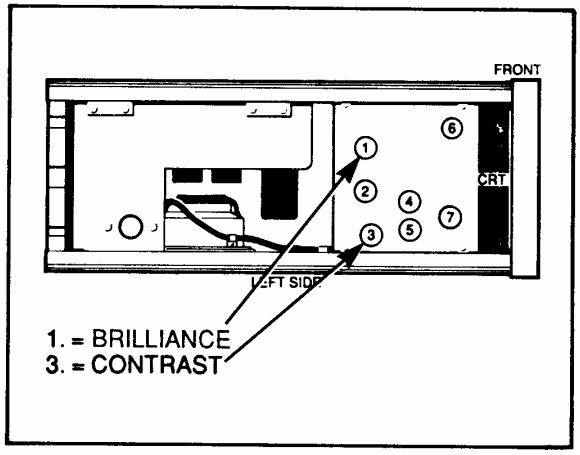


Figure 6-12. CRT Adjustments

c. Using the control panel intensity knob, you should now be able to reduce the screen intensity to a faint display.

SECTION VII
PARTS LISTS

SECTION VII
PARTS LISTS

7-1 INTRODUCTION

This section contains replaceable parts lists and data for the Models 6407 and 6409 RF Analyzer.

7-2 PARTS ORDERING INFORMATION

Replaceable parts may be ordered either through your local representative or directly from:

WILTRON Company
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408) 778-2000
FAX: (408) 778-0239
TLX: 285227 WILTRON MH

When placing your order, give complete information including model and serial number of the instrument, the full part description, WILTRON part number, and the quantity required.

7-3 PCB EXCHANGE PROGRAM

WILTRON has an exchange program that includes the assemblies shown in Table 7-1. Upon request, WILTRON will immediately ship a replacement for any RF Analyzer PCB or assembly covered by this program. The customer has 30 days in which to return the defective part. Contact Customer Service to make arrangements for an exchange.

7-4 ABBREVIATIONS

The following abbreviations appear in the "DESCRIPTION" column of the WILTRON parts lists:

CC - Carbon Composition
MF - Metal Film
GC - Gold Contacts
CER - Ceramic
TANT - Tantalum

7-5 REPLACEABLE PARTS

The replaceable parts lists for the RF Analyzer are arranged as follows:

NOTE

A6U20 is a programmed EPROM, or Personality PROM, that is model and option dependent. Hence, no part number is listed. When ordering the A6U20 replacement IC, please include model, serial number, and option information for your RF Analyzer.

Table 7-1. Exchange Assemblies

QTY.	DESCRIPTION	WILTRON PART NO.
1	CONTROL PANEL PCB (A1)	D30040-3
1	SIGNAL CHANNEL PCB (A3)	D30002-3
1	ATTENUATOR	C30067
1	OSCILLATOR ASSEMBLY, 4.4 TO 6.6 GHZ	C18366
1	DOWN CONVERTER, 1 GHZ	C31456
1	DOWN CONVERTER, 2 GHZ	C31466
1	RF OUTPUT ASSEMBLY, 50 OHM	B15085
1	RF OUTPUT ASSEMBLY, 75 OHM	B15815
1	YIG AND ALC PCB ASSEMBLY (A4)	D30003-3
1	CENTRAL PROCESSOR UNIT PCB (A6)	D30005-3
1	GRAPHIC DISPLAY PROCESSOR PCB (A7)	D30004-3
1	GPIB OPTION 3 (A8)	C30039
1	PROGRAMMABLE ATTENUATOR.	C30067
1	ENCODER CONTROL ASSEMBLY	B30092
1	MONITOR ASSEMBLY	2000-150

Table 7-2. Mainframe

QTY.	DESCRIPTION	WILTRON PART NO.
2	BAIL, TILT	C13654
4	FOOT, BOTTOM	D13655
4	FOOT, REAR	D13656
1	COVER, SIDE, RIGHT	C30051
1	COVER, TOP	D30125
1	COVER, SIDE, LEFT	D30127
4	HANDLE, BRACKET, CHEST, STL, BRU	783-12
4	HANDLE, CAP, TRIM, STL, BRUSHED	783-11
2	HANDLE, STRAP, VINYL	783-100
1	PCB BOX ASSEMBLY	D30015
1	CABLE ASSY., BUS	D30091
1	CABLE ASSY., A1/P3 TO A4/P12	B30094
1	CABLE ASSY., , A4/P6 TO A9/P2	B30100
1	CABLE ASSY.,, A9/P1 TO A10/P5	B30104
1	CABLE ASSY., A10/P7 TO CRT PCB	C30110
1	CABLE ASSY., A10/P6 TO A11	B30109
1	CABLE ASSY., A1/P2 TO A11/P1	B30093

Table 7-3. Front Panel

QTY.	DESCRIPTION	WILTRON PART NO.
1	FRONT PANEL OVERLAY, 6407	C30043-1
1	FRONT PANEL OVERLAY, 6409	C30043-2
2	INPUT CONNECTOR, A,B	551-152
1	KNOB, INTENSITY POT	A30132
1	KNOB, ENCODER	C30967
1	BUTTON, PUSH, GREY, "1"	430-243
1	BUTTON, PUSH, GREY, "2"	430-242
1	BUTTON, PUSH, GREY, "3"	430-241
1	BUTTON, PUSH, GREY, "4"	430-240
1	BUTTON, PUSH, GREY, "5"	430-239
1	BUTTON, PUSH, GREY, "6"	430-238
1	BUTTON, PUSH, GREY, "7"	430-237
1	BUTTON, PUSH, GREY, "8"	430-236
1	BUTTON, PUSH, GREY, "9"	430-235
1	BUTTON, PUSH, GREY, "0"	430-234
1	BUTTON, PUSH, GREY, "."	430-233
1	BUTTON, PUSH, GREY, "_"	430-232
30	BUTTON, SMALL GREY	C8187-1
1	BUTTON, SMALL WHITE	C8187-2
1	BUTTON, SMALL RED	C8187-3
41	SWITCH, PUSH BUTTON, 1STA, MOME	430-131

Table 7-4. Rear Panel

QTY.	DESCRIPTION	WILTRON PART NO.
1	CABLE ASSY., A9/P3 TO I/P MOD	C30105
1	TRANSFORMER, POWER, ASSY., 50/60 HZ	C-30105
1	CONNECTOR, CONTACT HOUSING	551-659
1	CABLE ASSY., A10/P3 TO COMP	B30108
1	CABLE ASSY., PWR SW TO I/P M A	C30111
1	SWITCH, LINE, OFF-ON PP	430-139
2	BRACKET, PANEL ANTIVIBRATION	C30144
1	CABLE ASSY., RECP OPEN LEADS, 24"	806-5
1	GUARD, FINGER, 6" DIA, 4 SCREW	790-251
1	LINE MODULE (SEE PAGE 2-2, FIGURE 2-1.)	260-9
	FAN, AXIAL, 120 M 3/H, 115VAC	650-11
1	CONNECTOR, BULKHD, BNC F, 500HM	510-5
1	CABLE ASSY., A10/P4 TO CENT A	B30106
1	FILTER, FAN, 5.25" DIA, .40" THK	783-377

Table 7-5. A1 Control Panel PCB (D30040-3)

REF DES	DESCRIPTION	WILTRON PART NO.
C1	CAPACITOR,FXD,PEST,0.10µF,10%	210-30
C2	CAPACITOR,FXD,PEST,0.22µF,20%	210-18
C3	CAPACITOR,FXD,CER,0.1µF,20%,1	230-37
C4	CAPACITOR,FXD,CER,0.1µF,20%,1	230-37
C5	CAPACITOR,FXD,CER,0.1µF,20%,1	230-37
C6	CAPACITOR,FXD,CER,0.1µF,20%,1	230-37
C7	CAPACITOR,FXD,CER,0.1µF,20%,1	230-37
C8	CAPACITOR,FXD,CER,0.1µF,20%,1	230-37
C9	CAPACITOR,FXD,CER,0.1µF,20%,1	230-37
C10	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C11	CAPACITOR,FXD,CER,0.1µF,20%,1	230-37
C12	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C13	CAPACITOR,FXD,MICA,39pF,5%,500V	223-39
C14	CAPACITOR,FXD,MICA,39pF,5%,500V	223-39
CR1	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR2	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR3	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR4	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR5	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
DS1	INDICATOR,LED,YEL,PANEL	15-32
DS2	INDICATOR,LED,YEL,PANEL	15-32
DS3	INDICATOR,LED,RED,PANEL	15-31
DS4	INDICATOR,LED,YEL,PANEL	15-32
DS5	INDICATOR,LED,YEL,PANEL	15-32
DS6	INDICATOR,LED,YEL,PANEL	15-32
DS7	INDICATOR,LED,YEL,PANEL	15-32
DS8	INDICATOR,LED,YEL,PANEL	15-32
DS9	INDICATOR,LED,RED,PANEL	15-31
DS1	INDICATOR,LED,YEL,PANEL	15-32
DS1	INDICATOR,LED,YEL,PANEL	15-32
DS1	INDICATOR,LED,RED,PANEL	15-31
DS1	INDICATOR,LED,YEL,PANEL	15-32
DS1	INDICATOR,LED,RED,PANEL	15-31
P1	CONNECTOR,HEADER,2 ROW 0.1	551-570
P2	CONNECTOR,HEADER,1 ROW 0.1	551-567
P3	CONNECTOR,HEADER,1 ROW 0.1	551-566
P4	CONNECTOR,HEADER,1 ROW 0.1	551-566
Q1	TRANSISTOR,FET,J112,SI,VHF	20-17
Q2	TRANSISTOR,NPN,2N4410,SI,HIGH	20-2N4410
Q3	TRANSISTOR,NPN,2N4410,SI,HIGH	20-2N4410
Q4	TRANSISTOR,NPN,2N4410,SI,HIGH	20-2N4410
R1	RESISTOR,FXD,MF,20.5K,1%,0.25	110-20.5K-1
R2	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R3	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R4	RESISTOR,FXD,MF,20.5K,1%,0.25W	110-20.5K-1
R5	RESISTOR,FXD,CC,2.2M,5%,0.25W	101-2.2M-5
R6	RESISTOR,FXD,MF,187K,1%,0.25W	110-187K-1
R7	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R8	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R10	RESISTOR,FXD,MF,7.15K,1%,0.25W	110-7.15K-1
R11	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R12	RESISTOR,FXD,MF,7.15K,1%,0.25W	110-7.15K-1
R13	RESISTOR,FXD,MF,187K,1%,0.25W	110-187K-1
R14	RESISTOR,FXD,MF,287K,1%,0.25W	110-287K-1
R15	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R16	RESISTOR,FXD,MF,34.8K,1%,0.25W	110-34.8K-1
R17	RESISTOR,FXD,MF,6.81K,1%,0.25W	110-6.81K-1
R18	RESISTOR,FXD,MF,3.32K,1%,0.25W	110-3.32K-1
R19	RESISTOR,FXD,MF,5.62K,1%,0.25W	110-5.62K-1
R20	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R21	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R22	RESISTOR,FXD,MF,3.32K,1%,0.25W	110-3.32K-1
R23	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R24	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R25	RESISTOR,FXD,MF,3.32K,1%,0.25W	110-3.32K-1
R26	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R27	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R28	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R29	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R30	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R31	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R32	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R33	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R34	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R35	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R36	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R37	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R38	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R39	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R40	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R41	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R42	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R43	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R44	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R45	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R46	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R47	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R48	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R49	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R50	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R51	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R52	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R53	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R54	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R55	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R56	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
U1	IC,TTL,74LS148,SINGLE,8 TO 3	54-354
U2	IC,TTL,74LS148,SINGLE,8 TO 3	54-354
U3	IC,TTL,74LS74,DUAL,D FLIP FLOP	54-44
U4	IC,TTL,74LS244,OCTAL,BUFFER	54-143
U5	IC,TTL,74LS374,OCTAL,D FLIP FLOP	54-41
U6	IC,TTL,74LS374,OCTAL,D FLIP FLOP	54-41
U7	IC,TTL,74LS138,3 TO 8 DECODE	54-74LS138
U8	IC,TTL,74LS74,DUAL,D FLIP FLOP	54-44
U9	IC,OP AMP,OP27GP,SNGL	54-595
U10	IC,OP AMP,TLO72,DUAL	354-53

Table 7-6. A3 Signal Channel PCB (D30002-3)

REF DES	DESCRIPTION	WILTRON PART NO.
C2	CAPACITOR,FXD,CER,2000pF,20%,5V	230-33
C3	CAPACITOR,FXD,PEST,1.0µF,10%,2V	210-36
C4	CAPACITOR,FXD,PEST,1.0µF,10%,2V	210-36
C5	CAPACITOR,FXD,PEST,0.022µFD,10V	210-38
C6	CAPACITOR,FXD,PEST,0.022µFD,10V	210-38
C7	CAPACITOR,FXD,MICA,680pF,5%,30V	220-680
C8	CAPACITOR,FXD,CER,2000pF,20%,5V	230-33
C9	CAPACITOR,FXD,CER,1000pF	230-30
C11	CAPACITOR,FXD,PEST,1.0µF,10%,2V	210-36
C12	CAPACITOR,FXD,PEST,1.0µF,10%,2V	210-36
C13	CAPACITOR,FXD,PEST,0.01µFD,10%	210-20
C14	CAPACITOR,FXD,CER,2000pF,20%,5V	230-33
C16	CAPACITOR,FXD,CER,1000pF	230-30
C17	CAPACITOR,FXD,CER,1000pF	230-30
C18	CAPACITOR,FXD,CER,1000pF	230-30
C19	CAPACITOR,FXD,CER,1000pF	230-30
C21	CAPACITOR,FXD,CER,0.05µF	230-35
C22	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C23	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C24	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C25	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C26	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C27	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C28	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C29	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C30	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C31	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C32	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C33	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C34	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C35	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C36	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42
C37	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C38	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42
C39	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C40	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42
C41	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C42	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C43	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C44	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C45	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C46	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C47	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42
C48	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C49	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C50	CAPACITOR,FXD,MICA,270pF,5%,50V	223-270
C51	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C52	CAPACITOR,FXD,CER,0.033µF,20%	230-32
C53	CAPACITOR,FXD,CER,0.033µF,20%	230-32
CR1	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR2	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR3	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR4	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR5	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR6	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR7	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR8	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR9	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR10	DIODE,ZENER,1N752A,5.6V,5%	10-1N752A
CR11	DIODE,ZENER,1N758A,10V,5%	10-1N758A
CR12	DIODE,ZENER,1N758A,10V,5%	10-1N758A
CR13	DIODE,ZENER,1N758A,10V,5%	10-1N758A
CR14	DIODE,ZENER,1N758A,10V,5%	10-1N758A
CR15	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR16	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR17	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR18	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR19	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
CR20	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446
J1	CONNECTOR,SOCKET,GOLD	551-577
P1	CONNECTOR,HEADER,1 ROW 0.1	551-567
P2	CONNECTOR,HEADER,1 ROW 0.1	551-567
P3	CONNECTOR,HEADER,2 ROW-0.1	551-570
P4	CONNECTOR,HEADER,1ROW 0.1	551-571
Q1	TRANSISTOR,FET,J112,SI,VHF,N,3	20-17
Q2	TRANSISTOR,FET,J112,SI,VHF,N,3	20-17
Q3	TRANSISTOR,FET,VN10K,VMOS,SING	20-57
Q4	TRANSISTOR,FET,VN10K,VMOS,SING	20-57
Q5	TRANSISTOR,FET,VN10K,VMOS,SING	20-57
Q6	TRANSISTOR,FET,J112,SI,VHF,N,3	20-17
Q7	TRANSISTOR,FET,J112,SI,VHF,N,3	20-17
Q8	TRANSISTOR,NPN,2N4410,SI,HIGH	20-2N4410
Q9	TRANSISTOR,NPN,2N4410,SI,HIGH	20-2N4410
R2	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R3	RESISTOR,FXD,CC,1M,5%,0.25W	101-1M-5
R4	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R5	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R6	RESISTOR,FXD,MF,46.4K,1%,0.25W	110-46.4K-1
R7	RESISTOR,FXD,MF,100,1%,0.25W	110-100-1
R9	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R10	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R11	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R12	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R13	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R14	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R15	RESISTOR,FXD,MF,12.7K,1%,0.25W	110-12.7K-1
R16	RESISTOR,FXD,MF,1.96K,1%,0.25W	110-1.96K-1
R17	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R18	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R19	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R20	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R21	RESISTOR,FXD,MF,5.11K,1%,0.25W	110-5.11K-1
R22	RESISTOR,FXD,MF,5.11K,1%,0.25W	110-5.11K-1
R23	RESISTOR,FIXED,METAL FILM	116-1.5M-5
R24	RESISTOR,FXD,MF,825K,1%,0.25W	110-825K-1
R25	RESISTOR,FXD,MF,825K,1%,0.25W	110-825K-1
R26	RESISTOR,FXD,MF,825K,1%,0.25W	110-825K-1
R27	RESISTOR,FXD,MF,825K,1%,0.25W	110-825K-1
R28	RESISTOR,FXD,MF,1.87K,1%,0.25W	110-1.87K-1
R29	RESISTOR,TRIM,CER,50K,10%,18T	157-50K-A
R30	RESISTOR,FXD,MF,1.47K,1%,0.25W	110-1.47K-1
R31	RESISTOR,TRIM,CER,20K,10%,18T	157-20K-A
R32	RESISTOR,FXD,MF,1.47K,1%,0.25W	110-1.47K-1
R33	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R34	RESISTOR,TRIM,CER,10K,10%,1T	156-10K-A
R35	RESISTOR,FXD,MF,95.3K,1%,0.25W	110-95.3K-1
R36	RESISTOR,FXD,MF,7.5K,1%,0.25W	110-7.5K-1
R37	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R38	RESISTOR,TRIM,CER,2K,10%,1T	156-2K-A
R39	RESISTOR,FXD,MF,42.2K,1%,0.25W	110-42.2K-1

Table 7-6. A3 Signal Channel PCB (D30002-3) Continued

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
R40	RESISTOR,FXD,MF,53.6K,1%,0.25WW	110-53.6K-1	R75	RESISTOR,FXD,MF,12.7K,1%,0.25W	110-12.7K-1
R41	RESISTOR,FXD,MF,10.5K,1%,0.25W	110-10.5K-1	R76	RESISTOR,TRIM,CER,200K,10%,1T	156-200K-A
R42	RESISTOR	156-200-A	R77	RESISTOR,TRIM,CER,200K,10%,1T	156-200K-A
R43	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1	R79	RESISTOR,FXD,MF,110,1%,0.25W	110-110-1
R44	RESISTOR,FIXED,METAL FILM	116-1.5M-5	U1	IC,OP AMP,(INSTRUMENTATION)	54-449
R45	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U2	IC,OP AMP,LF356,SNGL	50-9
R46	RESISTOR,FXD,CC,2.2M,5%,0.25W	101-2.2M-5	U3	IC,OP AMP,LF356,SNGL	50-9
R47	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U4	IC,ANALOG SWITCH,DG211,QUAD	54-208
R48	RESISTOR,FXD,CC,2.2M,5%,0.25W	101-2.2M-5	U5	IC,ANALOG SWITCH,DG211,QUAD	54-208
R49	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U6	IC,OP AMP,LF398,SNGL	54-204
R50	RESISTOR,FXD,MF,2K,1%,0.25W	110-2K-1	U7	IC,OP AMP,LF356,SNGL	50-9
R51	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U8	IC,A/D,574,12 BIT,BINARY,25uS	54-453
R52	RESISTOR,FXD,CC,1M,5%,0.25W	101-1M-5	U9	IC, CALL FACTORY	
R53	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U10	IC,TTL,74LS244,OCTAL,BUFFER	54-143
R54	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1	U11	IC,TTL,74LS244,OCTAL,BUFFER	54-143
R55	RESISTOR,FXD,MF,100,1%,0.25W	110-100-1	U12	IC,TTL,74LS244,OCTAL,BUFFER	54-143
R56	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U13	IC,D/A,AD7524,8BITS,BINARY	54-129
R57	RESISTOR,FXD,MF,15.4K,1%,0.25W	110-15.4K-1	U14	IC,OP AMP,LF356,SNGL	50-9
R58	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U15	IC,OP AMP,LF356,SNGL	50-9
R59	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U16	IC,TTL,74LS374,OCTAL,D FLIP FLOP	54-41
R60	RESISTOR,FXD,MF,3.32K,1%,0.25W	110-3.32K-1	U17	IC,TTL,74LS374,OCTAL,D FLIP FLOP	54-41
R61	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1	U18	IC,TTL,74LS138,3 TO 8 DECODE	54-74LS138
R62	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U19	IC,TTL,74LS138,3 TO 8 DECODE	54-74LS138
R63	RESISTOR,FXD,MF,100,1%,0.25W	110-100-1	U20	IC,TTL,74LS374,OCTAL,D FLIP FLOP	54-41
R64	RESISTOR,FXD,MF,3.83K,1%,0.25W	110-3.83K-1	U21	IC,VOLTAGE REGULATOR,78LO5,5V	54-451
R65	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U22	IC,ANALOG SWITCH,DG211,QUAD	54-208
R66	RESISTOR,FXD,MF,3.32K,1%,0.25W	110-3.32K-1	U23	IC,ANALOG SWITCH,13201,QUAD	54-20
R67	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1	U24	IC,ANALOG SWITCH,200,DUAL,15V	54-450
R68	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U25	IC,ANALOG SWITCH,200,DUAL,15V	54-450
R69	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U26	IC,TTL,74LS04,HEX,INVERTERS	54-74LS04
R70	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1	U27	IC,OP AMP,TL074CN3,QUAD	54-132
R71	RESISTOR,TRIM,CER,2K,10%,1T	158-16	U28	IC,OP AMP,TL074CN3,QUAD	54-132
R72	RESISTOR,FXD,MF,56.2,1%,0.25W	110-56.2-1	U29	IC,ANALOG SWITCH,200,DUAL,15V	54-450
R73	RESISTOR,FXD,MF,56.2,1%,0.25W	110-56.2-1	U30	IC,OP AMP,TLO72,DUAL	54-53
R74	RESISTOR,FXD,MF,1.96K,1%,0.25W	110-1.96K-1			

Table 7-7. A4 A4 Sweeper PCB (D30003-3)

REF DES	DESCRIPTION	WILTRON PART NO.
C1	CAPACITOR,FXD,TANT,68µF,10%,6V	250-58A
C2	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C5	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C6	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C7	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C8	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C9	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C10	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C11	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C12	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C13	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C15	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C16	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C17	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C18	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C19	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C20	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C21	CAPACITOR,FXD,CER,470pF,10%,10V	223-470
C22	CAPACITOR,FXD,CER,470pF,10%,10V	223-470
C23	CAPACITOR,FXD,CER,470pF,10%,10V	223-470
C24	CAPACITOR,FXD,CER,470pF,10%,10V	223-470
C25	CAPACITOR,FXD,CER,0.01µF	230-11
C26	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42
C27	CAPACITOR,FXD,CER,0.01µF	230-11
C28	CAPACITOR,FXD,MICA,12pF,5%,500V	220-12
C29	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C30	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C31	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42
C32	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42
C33	CAPACITOR,FXD,CER,0.01µF	230-11
C34	CAPACITOR,FXD,CER,1000pF	230-30
C35	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C36	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C37	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C38	CAPACITOR,FIXED,STRONTIUM	250-132
C39	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C40	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C41	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C42	CAPACITOR,FIXED,STRONTIUM	250-131
C43	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C44	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C45	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C46	CAPACITOR,FXD,TANT,4.7µF,20%,3V	250-39A
C47	CAPACITOR,FXD,CER,1000pF	230-30
C48	CAPACITOR,FXD,CER,1000pF	230-30
C50	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42
C51	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C52	CAPACITOR,FXD,TANT,2.2µF,20%,2V	250-40A
C53	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C54	CAPACITOR,FXD,TANT,2.2µF,20%,2V	250-40A
C55	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C56	CAPACITOR,FXD,TANT,2.2µF,20%,2V	250-40A
C57	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C58	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C59	CAPACITOR,FXD,MICA,39pF,5%,500V	223-39
C62	CAPACITOR,FXD,MICA,39pF,5%,500V	223-39
C63	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C64	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C65	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C66	CAPACITOR,FXD,MICA,3pF,0.5pF,5V	223-3
C67	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C68	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C69	CAPACITOR,FXD,CER,1000pF	230-30
C70	CAPACITOR,FXD,CER,0.01µF	230-11
C71	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C72	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C73	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C74	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C83	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42
C84	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19A
C85	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C86	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C87	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C88	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C89	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C90	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C91	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C92	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C93	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C94	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C95	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C96	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C97	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C98	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C99	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C100	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C101	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C102	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C103	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C104	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C105	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37
C106	CAPACITOR,FXD,CER,0.1µF,20%,10V	10-1N751A
C107	CAPACITOR,FXD,CER,0.1µF,20%,10V	10-1N751A
C108	CAPACITOR,FXD,CER,0.1µF,20%,10V	10-1N751A
C109	CAPACITOR,FXD,CER,0.1µF,20%,10V	10-1N751A
C110	CAPACITOR,FXD,CER,0.1µF,20%,10V	10-1N751A
C111	CAPACITOR,FXD,CER,0.1µF,20%,10V	10-1N751A
CR1	DIODE,RECTIFIER,IN4003,200V	10-SI2
CR2	DIODE,RECTIFIER,IN4003,200V	10-SI2
CR3	DIODE,ZENER,1N827,6.2V,5%	10-1N827
CR4	DIODE RECTIFIER,IN3595,125V,4A	10-FD300
CR5	DIODE RECTIFIER,IN3595,125V,4A	10-FD300
CR6	DIODE,ZENER,1N750A,4.7V,10%	10-11
CR7	DIODE,ZENER,1N750A,4.7V,10%	10-11
CR8	DIODE,RECTIFIER,IN4148,75V	10-60
CR9	DIODE,RECTIFIER,IN4148,75V	10-60
CR10	DIODE,RECTIFIER,IN4003,200V	10-SI2
CR11	DIODE,ZENER,1N4749,24V,10%	10-1N4749A
CR12	DIODE,RECTIFIER,IN4003,200V	10-SI2
CR14	DIODE,RECTIFIER,IN4148,75V	10-60
CR15	DIODE,RECTIFIER,IN4148,75V	10-60
CR16	DIODE,RECTIFIER,IN4148,75V	10-60
CR17	DIODE,RECTIFIER,IN4148,75V	10-60
CR18	DIODE,RECTIFIER,IN4148,75V	10-60
CR19	DIODE,RECTIFIER,IN4148,75V	10-60
CR20	DIODE,RECTIFIER,IN4148,75V	10-60
CR21	DIODE,RECTIFIER,IN4148,75V	10-60
CR22	DIODE,RECTIFIER,IN4148,75V	10-60
CR23	DIODE,RECTIFIER,IN4148,75V	10-60
CR24	DIODE,RECTIFIER,IN4148,75V	10-60
CR25	DIODE,RECTIFIER,IN4148,75V	10-60
CR26	DIODE,RECTIFIER,IN4148,75V	10-60
CR27	DIODE,RECTIFIER,IN4148,75V	10-60

Table 7-7. A4 Sweeper PCB (D30003-3) Continued

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
CR28	DIODE,RECTIFIER,IN4148,75V	10-60	R1	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
CR29	DIODE,RECTIFIER,IN4148,75V	10-60	R2	RESISTOR,FXD,MF,20K,1%,0.25W	110-20K-1
CR30	DIODE,RECTIFIER,IN4148,75V	10-60	R3	RESISTOR,FXD,MF,12.7K,1%,0.25W	110-12.7K-1
CR31	DIODE,RECTIFIER,IN4148,75V	10-60	R4	RESISTOR,TRIM,CER,1K,10%,18T	157-1K-A
CR32	DIODE,RECTIFIER,IN4148,75V	10-60	R5	RESISTOR,TRIM,CER,20K,10%,18T	54-595
CR33	DIODE,ZENER,1N752A,5.6V,5%	10-1N752A	R6	RESISTOR,TRIM,CER,20K,10%,18T	54-595
CR34	DIODE,ZENER,1N752A,5.6V,5%	10-1N752A	R7	RESISTOR,TRIM,CER,20K,10%,18T	54-595
CR35	DIODE,RECTIFIER,IN4148,75V	10-60	R8	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
CR36	DIODE,RECTIFIER,IN4003,200V	10-SI2	R9	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
CR37	DIODE,RECTIFIER,IN3595,125V,4A	10-FD300	R11	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
CR38	DIODE,RECTIFIER,IN3595,125V,4A	10-FD300	R13	RESISTOR,FXD,MF,6.49K,1%,0.25W	110-6.49K-1
CR39	DIODE,ZENER,1N823,6.2V,5%	10-1N823	R14	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
CR40	DIODE,RECTIFIER,IN3595,125V,4A	10-FD300	R15	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
CR41	DIODE,RECTIFIER,IN3595,125V,4A	10-FD300	R16	RESISTOR,TRIM,CER,5K,10%,18T	157-5K-A
CR42	DIODE,RECTIFIER,IN3595,125V,4A	10-FD300	R17	RESISTOR,FXD,MF,12.1K,1%,0.25W	110-12.1K-1
CR43	DIODE,RECTIFIER,IN3595,125V,4A	10-FD300	R18	RESISTOR,TRIM,CER,10K,10%,18T	157-10K-A
CR45	DIODE,RECTIFIER,IN4148,75V	10-60	R19	RESISTOR,FXD,MF,20K,1%,0.25W	110-20K-1
CR53	DIODE,RECTIFIER,IN4003,200V	10-SI2	R20	RESISTOR,TRIM,CER,10K,10%,18T	157-10K-A
CR54	DIODE,RECTIFIER,IN4003,200V	10-SI2	R21	RESISTOR,FXD,MF,15K,1%,0.25W	110-15K-1
CR55	DIODE,RECTIFIER,IN4003,200V	10-SI2	R22	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
CR56	DIODE,ZENER,1N751A,5.1V,5%	10-1N751A	R25	RESISTOR,FXD,MF,51.1,1%,0.25W	110-51.1-1
CR57	DIODE,RECTIFIER,IN4148,75V	10-60	R26	RESISTOR,FXD,MF,51.1,1%,0.25W	110-51.1-1
J1	CONNECTOR,SOCKET,GOLD	551-577	R27	RESISTOR,FXD,MF,5.11,1%,0.25W	110-5.11-1
J2	CONNECTOR,SOCKET,GOLD	551-577	R28	RESISTOR,FXD,MF,82.5,1%,0.25W	110-82.5-1
J3	CONNECTOR,SOCKET,GOLD	551-577	R29	RESISTOR,FXD,MF,82.5,1%,0.25W	110-82.5-1
P1	CONNECTOR,HEADER,2 ROW-0.1	551-564	R30	RESISTOR,FXD,MF,3.65K,1%,0.25W	110-3.65K-1
P3	CONNECTOR,HEADER,1 ROW 0.1	551-567	R31	RESISTOR,FXD,MF,3.65K,1%,0.25W	110-3.65K-1
P4	CONNECTOR,HEADER,1ROW-0.98	551-533	R32	RESISTOR,FXD,MF,31.6,1%,0.25W	110-31.6-1
P5	CONNECTOR,HEADER,1 ROW 0.1	551-567	R33	RESISTOR,FXD,MF,31.6,1%,0.25W	110-31.6-1
P6	CONNECTOR,HEADER,1 ROW-0.1	551-573	R34	RESISTOR,FXD,MF,31.6,1%,0.25W	110-31.6-1
P7	CONNECTOR,HEADER,1 ROW-0.1	551-573	R35	RESISTOR,FXD,MF,31.6,1%,0.25W	110-31.6-1
P8	CONNECTOR,HEADER,1 ROW 0.1	551-567	R36	RESISTOR,FXD,MF,121,1%,0.25W	110-121-1
P12	CONNECTOR,HEADER,1 ROW 0.1	551-566	R37	RESISTOR,FXD,MF,121,1%,0.25W	110-121-1
P13	CONNECTOR,HEADER,1ROW 0.1	551-571	R38	RESISTOR,FXD,MF,121,1%,0.25W	110-121-1
P14	CONNECTOR,HEADER,1ROW 0.1	551-571	R39	RESISTOR,FXD,MF,121,1%,0.25W	110-121-1
P15	CONNECTOR,HEADER,1 ROW 0.1	551-569	R40	RESISTOR,TRIM,CER,10K,10%,18T	157-10K-A
P16	CONNECTOR,HEADER,1 ROW 0.1	551-569	R41	RESISTOR,FXD,MF,75K,1%,0.25W	110-75K-1
Q2	TRANSISTOR,PNP,2N6041,SI,DARLI	20-2N6041	R42	RESISTOR,FXD,MF,110K,1%,0.25W	110-110K-1
Q3	TRANSISTOR,PNP,MPSA92,SI,HIGH	20-MPSA92	R43	RESISTOR,TRIM,CER,20K,10%,18T	157-20K-A
Q4	TRANSISTOR,NPN,2N6044,SI,DARLI	20-2N6044	R44	RESISTOR,FXD,MF,140K,1%,0.25W	110-140K-1
Q8	TRANSISTOR,PNP,2N2907A,SI,MED	20-2N2907	R45	RESISTOR,FXD,MF,147K,1%,0.25W	110-147K-1
Q9	TRANSISTOR,NPN,2N2222A,SI,MED	20-2N2222A	R46	RESISTOR,TRIM,CER,5K,10%,18T	157-5K-A
Q10	TRANSISTOR,PNP,2N2907A,SI,MED	20-2N2907	R47	RESISTOR,FXD,MF,46.4K,1%,0.25W	110-46.4K-1
Q11	TRANSISTOR,NPN,2N6044,SI,DARLI	20-2N6044	R48	RESISTOR,FXD,MF,42.2K,1%,0.25W	110-42.2K-1
Q12	TRANSISTOR,NPN,MPSA42,SI,HIGH	20-MPSA42	R49	RESISTOR,FXD,WW,5,3%,5W,3PPM	131-3
Q13	TRANSISTOR,PNP,MPSA92,SI,HIGH	20-MPSA92	R50	RESISTOR,FXD,MF,7.87K,1%,0.25W	110-7.87K-1
Q14	TRANSISTOR,PNP,TIP117,SI,PWR D	20-5	R51	RESISTOR,FXD,MF,511,1%,0.25W	110-511-1
Q15	TRANSISTOR,PNP,MPSA92,SI,HIGH	20-MPSA92	R52	RESISTOR,FXD,MF,511,1%,0.25W	110-511-1
Q16	TRANSISTOR,PNP,2N2907A,SI,MED	20-2N2907	R53	RESISTOR,FXD,MF,2K,1%,0.25W	110-2K-1
Q18	TRANSISTOR,NPN,2N3694,SI,GEN	20-2N3694	R54	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
Q19	TRANSISTOR,FET,VN10K,VMOS,SING	20-57	R55	RESISTOR,FXD,MF,121,1%,0.25W	110-121-1
Q20	TRANSISTOR,FET,VN10K,VMOS,SING	20-57	R56	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
Q21	TRANSISTOR,PNP,MPSA92,SI,HIGH	20-MPSA92	R57	RESISTOR,FXD,MF,2K,1%,0.25W	110-2K-1
Q22	TRANSISTOR,FET,VN10K,VMOS,SING	20-57	R58	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
Q23	TRANSISTOR,FET,VN10K,VMOS,SING	20-57	R58	RESISTOR,FXD,MF,7.5K,1%,0.25W	110-7.5K-1
Q24	TRANSISTOR,PNP,MPSA92,SI,HIGH	20-MPSA92	R60	RESISTOR,FXD,MF,5.11K,1%,0.25W	110-5.11K-1
Q25	TRANSISTOR,PNP,MPSA92,SI,HIGH	20-MPSA92	R63	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
Q28	TRANSISTOR,PNP,2N2907A,SI,MED	20-2N2907	R68	RESISTOR,FXD,MF,30.1K,1%,0.25W	110-30.1K-1
Q29	TRANSISTOR,NPN,2N2222A,SI,MED	20-2N2222A	R69	RESISTOR,FXD,MF,11K,1%,0.25W	110-11K-1
Q30	TRANSISTOR,PNP,2N2907A,SIK,MED	20-2N2907	R70	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
Q31	TRANSISTOR,NPN,2N2222A,SI,MED	20-2N2222A	R71	RESISTOR,FXD,MF,3.16K,1%,0.25W	110-3.16K-1

Table 7-7. A4 Sweeper PCB (D30003-3) Continued

REF DES	DESCRIPTION	WILTRON PART NO.
R72	RESISTOR,FXD,MF,3.16K,1%,0.25W	110-3.16K-1
R73	RESISTOR,FXD,MF,511,1%,0.25W	110-511-1
R74	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R75	RESISTOR,FXD,MF,511,1%,0.25W	110-511-1
R76	RESISTOR,FXD,MF,2.74K,1%,0.25W	110-2.74K-1
R77	RESISTOR,FXD,MF,5.11,1%,0.25W	110-5.11-1
R78	RESISTOR,FXD,MF,5.11,1%,0.25W	110-5.11-1
R79	RESISTOR,FXD,MF,196,1%,0.25W	110-196-1
R80	RESISTOR,FXD,MF,4.42K,1%,0.25W	110-4.42K-1
R81	RESISTOR,FXD,MF,1.21K,1%,0.25W	110-1.21K-1
R82	RESISTOR,FXD,MF,681,1%,0.25W	110-681-1
R83	RESISTOR,FXD,MF,1.47K,1%,0.25W	110-1.47K-1
R84	RESISTOR,FXD,MF,1.47K,1%,0.25W	110-1.47K-1
R85	RESISTOR,FXD,MF,38.3, 1%,0.25W	110-38.3-1
R85	RESISTOR,FXD,MF,38.3,1%,0.25W	110-38.3-1
R86	RESISTOR,FXD,CC,2.2K,5%,0.5W	102-2.2K-5
R87	RESISTOR,FXD,MF,590,1%,0.25W	110-590-1
R88	RESISTOR,FIXED,WIREWOUND,0.47	130-.47-3
R89	RESISTOR,FXD,MF,200K,1%,0.25W	110-200K-1
R90	RESISTOR,FXD,MF,316K,1%,0.25W	110-316K-1
R93	RESISTOR,FXD,CC,1M,5%,0.25W	101-1M-5
R94	RESISTOR,FXD,MF,511K,1%,0.25W	110-511K-1
R95	RESISTOR,FXD,MF,511K,1%,0.25W	110-511K-1
R96	RESISTOR,FXD,MF,511K,1%,0.25W	110-511K-1
R97	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R98	RESISTOR,FXD,MF,36.5K,1%,0.25W	110-36.5K-1
R99	RESISTOR,FXD,MF,30.1K,1%,0.25W	110-30.1K-1
R100	RESISTOR,FXD,MF,30.1K,1%,0.25W	110-30.1K-1
R102	RESISTOR,FXD,MF,2.49K,1%,0.25W	110-2.49K-1
R103	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R104	RESISTOR,FXD,MF,40.2K,1%,0.25W	110-40.2K-1
R105	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R106	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R107	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R108	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R109	RESISTOR,FXD,MF,20K,1%,0.25W	110-20K-1
R110	RESISTOR,FXD,MF,825,1%,0.25W	110-825-1
R111	RESISTOR,FXD,MF,2.87K,1%,0.25W	110-2.87K-1
R112	RESISTOR,FXD,MF,2K,1%,0.25W	110-2K-1
R113	RESISTOR,TRIM,CER,20K,10%,18T	157-20K-A
R114	RESISTOR,TRIM,CER,100K,10%,18	157-100K-A
R115	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R116	RESISTOR,FXD,MF,511,1%,0.25W	110-511-1
R117	RESISTOR,FXD,MF,511,1%,0.25W	110-511-1
R118	RESISTOR,FXD,MF,2.49K,1%,0.25W	110-2.49K-1
R119	RESISTOR,FXD,MF,2.49K,1%,0.25W	110-2.49K-1
R120	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R121	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R121	RESISTOR,FXD,MF,4.42K,1%,0.25W	110-4.42K-1
R122	RESISTOR,FXD,MF,5.11K,1%,0.25W	110-5.11K-1
R123	RESISTOR,FXD,MF,5.11K,1%,0.25W	110-5.11K-1
R124	RESISTOR,FXD,MF,15K,1%,0.25W	110-15K-1
R125	RESISTOR,FIXED,WIREWOUND,270	130-270-3
R126	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R129	RESISTOR,FXD,MF,15K,1%,0.25W	110-15K-1
R130	RESISTOR,FXD,MF,4.64K,1%,0.25W	110-4.64K-1
R131	RESISTOR,FXD,MF,3.01K,1%,0.25W	110-3.01K-1
R132	RESISTOR,FXD,MF,3.01K,1%,0.25W	110-3.01K-1
R133	RESISTOR,FXD,MF,12.1K,1%,0.25W	110-12.1K-1
R134	RESISTOR,FXD,MF,511,1%,0.25W	10-511-1
R136	RESISTOR,FXD,MF,511,1%,0.25W	110-511-1
R137	RESISTOR,TRIM,CER,20K,10%,18T	157-20K-A
R138	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R139	RESISTOR,FXD,MF,511K,1%,0.25W	110-511K-1
R140	RESISTOR,TRIM,CER,50K,10%,18T	157-50K-A
R141	RESISTOR,FXD,MF,511,1%,0.25W	110-511-1
R142	RESISTOR,FXD,MF,511,1%,0.25W	110-511-1
R154	RESISTOR,FXD,CC,1M,5%,0.25W	101-1M-5
R155	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R156	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R157	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R158	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R159	RESISTOR,FXD,CC,1M,5%,0.25W	101-1M-5
R160	RESISTOR,FXD,CC,1M,5%,0.25W	101-1M-5
R161	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R162	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R174	RESISTOR,FXD,MF,237,1%,0.25W	110-237-1
R175	RESISTOR,FXD,MF,1.47K,1%,0.25W	110-1.47K-1
R176	RESISTOR,FXD,MF,5.11K,1%,0.25W	110-5.11K
R177	RESISTOR,FXD,MF,15K,1%,0.25W	110-15K-1
R178	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R179	RESISTOR,FXD,MF,750,1%,0.25W	110-750-1
R180	RESISTOR,FXD,MF,5.9K,1%,0.25W	110-5.9K-1
R181	RESISTOR,FXD,MF,15K,1%,0.25W	110-15K-1
R182	RESISTOR,FXD,CC,560,5%,0.5W	102-560-5
R183	RESISTOR,FXD,MF,3.32K,1%,0.25W	110-3.32K-1
R184	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R185	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R186	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R187	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R188	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R189	RESISTOR,TRIM,CER,10K,10%,18T	157-10K-A
R190	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
R191	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
R192	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
R194	RESISTOR,FXD,CC,10M,5%,0.25W	101-10M-5
R195	RESISTOR,TRIM,CER,20K,10%,18T	54-595
R196	RESISTOR,FXD,MF,3.16K,1%,0.25W	110-3.16K-1
R198	RESISTOR,FXD,MF,3.16K,1%,0.25W	110-3.16K-1
R199	RESISTOR,FXD,MF,499K,1%,0.25W	110-499K-1
R200	RESISTOR,FXD,MF,2.21K,1%,0.25W	110-2.21K-1
R201	RESISTOR,FXD,CC,1M,5%,0.25W	101-1M-5
U1	IC,TTL,74LS374,OCTAL,D FLIP FLOP	54-41
U2	IC,TTL,74LS374,OCTAL,D FLIP FLOP	54-41
U3	IC,TTL,74LS174,HEX,D FLIP FLOP	54-43
U4	IC,TTL,74LS32,QUAD,2 INPUT OR	54-74LS32
U5	IC,TTL,74LS138,3 TO 8 DECODE	54-74LS138
U6	IC,TTL,74LS04,HEX,INVERTERS	54-74LS04
U7	IC,TTL,74LS138,3 TO 8 DECODE	54-74LS138
U8	IC,TTL,74LS138,3 TO 8 DECODE	54-74LS138
U9	IC,TTL,74LS174,HEX,D FLIP FLOP	54-43
U10	IC,TTL,74LS175,QUAD,D FLIP FLOP	54-74LS175
U11	IC,D/A,AD7533,10BIT,BINARY	54-593
U12	IC,TTL,74LS174,HEX,D FLIP FLOP	54-43
U13	IC,TTL,74LS175,QUAD,D FLIP FLOP	54-74LS175
U14	IC,D/A,AD7533,10BIT,BINARY	54-593
U15	IC,TTL,74LS174,HEX,D FLIP FLOP	54-43
U16	IC,TTL,74LS175,QUAD,D FLIP FLOP	54-74LS175
U17	IC,D/A,AD7533,10BIT,BINARY	54-593
U18	IC,D/A,AD7545,12 BIT,BINARY	54-432
U19	IC,OP AMP,OP27G	54-595
U20	IC,OP AMP,LF356	50-9

Table 7-7. A4 Sweeper PCB (D30003-3) Continued

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
U21	IC,OP AMP,OP27G	54-595	U37	IC,TTL,74LS175,QUAD,D FLIP FLOP	54-74LS175
U22	IC,OP AMP,OP27G	54-595	U38	IC,D/A,AD7533,10BIT,BINARY	54-593
U23	IC,OP AMP,OP27G	54-595	U39	IC,D/A,AD7533,10BIT,BINARY	54-593
U24	IC,OP AMP,TL074CN3,QUAD	54-132	U40	IC,OP AMP,TL074CN3,QUAD	54-132
U25	IC,ANALOG SWITCH,13201,QUAD	54-20	U41	IC,OP AMP,TL074CN3,QUAD	54-132
U26	IC,OP AMP,NE530	50-7	U42	IC,OP AMP,NE530	50-9
U27	IC,OP AMP,OPO5	54-87	U43	IC,OP AMP,LF357	50-7
U28	IC,OP AMP,TL071	54-433	U44	IC,TTL,74LS00,QUAD,2 INPUT NAN	54-74LS00
U29	IC,TTL,75451,DUAL,PERIPHERAL	54-144	U45	IC,ANALOG SWITCH,13201,QUAD	54-20
U30	IC,TTL,75451,DUAL,PERIPHERAL	54-144	U46	IC,OP AMP,LF356	50-9
U31	IC,TTL,75451,DUAL,PERIPHERAL	54-144	U47	IC,OP AMP,LF356	50-9
U32	IC,TTL,75451,DUAL,PERIPHERAL	54-144	U48	IC,OP AMP,LF356	50-9
U33	IC,VOLTAGE REGULATOR,7815,15V	54-MC7815CP	U49	IC,OP AMP,LF356	50-9
U34	IC,VOLTAGE REGULATOR,7915,-15V	54-MC7915CP	U51	IC,VOLTAGE REG,78L12,+12V,+35V	54-434
U35	IC,VOLTAGE REGULATOR,LM317,1.2	54-333	U52	IC,TTL,74LS367,HEX,BUS DRIVERS	54-74LS367
U36	IC,TTL,74LS174,HEX,D FLIP FLOP	54-43	U53	IC,TTL,74LS74,DUAL,D FLIP FLOP	54-44

Table 7-8. A6 CPU PCB (D30005-3)

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
B1	BATTERY,NICD,2.4V	633-8	R8	RESISTOR,FXD,MF,274K,1%,0.25	110-274K-1
C1	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42	R9	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
C2	CAPACITOR,FXD,TANT,150µF,10%,6V	250-57	R10	RESISTOR,FXD,MF,10K,1%,0.25	110-10K-1
C3	CAPACITOR,FXD,TANT,10µF,10%,25V	250-42	R11	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
C4	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R12	RESISTOR,FXD,MF,1M,1%,0.25W	110-1M-1
C5	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R13	RESISTOR,FXD,MF,422,1%,0.25W	110-422-1
C7	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R14	RESISTOR,FXD,MF,4.87K,1%,0.25W	110-4.87K-1
C8	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R15	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
C9	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R16	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
C10	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R17	RESISTOR,FXD,MF,2K,1%,0.25W	110-2K-1
C11	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R18	RESISTOR,FXD,MF,2K,1%,0.25W	110-2K-1
C12	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R19	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
C13	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R20	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
C14	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R21	RESISTOR,FXD,MF,348K,1%,0.25W	110-348K-1
C15	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R22	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C16	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R23	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C17	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R24	RESISTOR,FXD,MF,16.5K,1%,0.25W	110-16.5K-1
C18	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R25	RESISTOR,FXD,MF,274K,1%,0.25W	110-274K-1
C19	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R26	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1
C20	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R27	RESISTOR,FXD,MF,422,1%,0.25W	110-422-1
C21	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R28	RESISTOR,FXD,MF,51.1,1%,0.25W	110-51.1-1
C22	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R29	RESISTOR,TRIM,CER,100K,10%,1T	158-6
C23	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R30	RESISTOR,TRIM,CER,100K,10%,1T	158-6
C24	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R31	RESISTOR,FXD,MF, 22.6K,1%,0.25W	110-22.6K-1
C25	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R32	RESISTOR,FXD,MF, 22.6K,1%,0.25W	110-22.6K-1
C26	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	U1	IC,MICROPROCESSOR,8088-2	54-320
C27	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19	U2	IC,MICROPROCESSOR,8284A	54-317
C28	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19	U3	IC,TTL,74LS74,DUAL,D FLIP FLOP	54-44
C29	CAPACITOR,FXD,CER,0.05µF	230-35	U4	IC,TTL,74LS373,OCTAL,TRANSPARE	54-103
C30	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	U5	IC,TTL,74LS138,3 TO 8 DECODE	54-74LS138
C31	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	U6	IC,TTL,74LS32,QUAD,2 INPUT OR	54-74LS32
C32	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	U7	IC,TTL,74LS138,3 TO 8 DECODE	54-74LS138
C33	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	U8	IC,TTL,74LS244,OCTAL,BUFFER	54-143
C34	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	U9	IC,TTL,74LS245,OCTAL BIDIREC	54-344
C35	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19	U10	IC,TTL,74LS00,QUAD,2 INPUT NAN	54-74LS00
C36	CAPACITOR,FXD,TANT,1µF,10%,35V	250-19	U11	IC,TTL,74LS244,OCTAL,BUFFER	54-143
CR1	DIODE,RECTIFIER,IN4003,200V	10-SI2	U12	IC,TTL,74LS08,QUAD,2 INPUT AND	54-74LS08
CR2	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	U13	IC, CALL FACTORY	
CR3	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	U14	IC, CALL FACTORY	
CR4	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	U15	IC, CALL FACTORY	
CR5	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	U16	IC, CALL FACTORY	
J1	CONNECTOR,SOCKET,GOLD	551-577	U17	IC MEMORY,HM6264LP,RAM,8K/8	54-455
P1	CONNECTOR,HEADER,1 ROW 0.1",	551-569	U18	IC MEMORY,HM6264LP,RAM,8K/8	54-455
Q1	TRANSISTOR,PNP,MJE371,SI,MED P	20-24	U19	IC, CALL FACTORY	
Q2	TRANSISTOR,NPN,2N2222A,SI,MED	20-2N2222A	U20	IC, CALL FACTORY	
Q3	TRANSISTOR,NPN,2N2222A,SI,MED	20-2N2222A	U21	IC,OP AMP,ICL8212	54-151
Q4	TRANSISTOR,NPN,2N2222A,SI,MED	20-2N2222A	U22	IC,TTL,74LS244,OCTAL,BUFFER	54-143
Q5	TRANSISTOR,NPN,2N2222A,SI,MED	20-2N2222A	U23	IC,TTL,74LS148,SINGLE,8 TO 3	54-354
R1	RESISTOR,FXD,MF,100K,1%,0.25W	110-100K-1	U24	IC,TTL,74LS73,DUAL,JK FLIP FLOP	54-74LS73
R3	RESISTOR,FXD,MF,12.1K,1%,0.25W	110-12.1K-1	U25	IC,TTL,74LS112,DUAL,JK FLIP FLOP	54-74LS112
R4	RESISTOR,FXD,MF,46.4K,1%,0.25W	110-46.4K-1	U26	IC,TTL,74LS132,QUAD,NAND SCHMIDT	54-74LS132
R5	RESISTOR,FXD,MF,147,1%,0.25W	110-147-1	U27	IC,OP AMP,LF356	50-9
R6	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U28	IC,OP AMP,ICL8212	54-151
R7	RESISTOR,FXD,MF,20.5K,1%,0.25W	110-20.5K-1	X1	CRYSTAL,14.31818MHz,0.002%	630-35

Table 7-9. A7 GDP PCB (D30004-3)

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
C1	CAPACITOR,FXD,MICA,82pF,5%,500V	223-82	R15	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C2	CAPACITOR,FXD,TANT,10pF,10%,25V	250-42	R16	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1
C3	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R17	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1
C4	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R18	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1
C5	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R19	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1
C7	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R20	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1
C11	CAPACITOR,FXD,TANT,10pF,10%,25V	250-42	R21	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1
C12	CAPACITOR,FXD,TANT,10pF,10%,25V	250-42	R22	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C13	CAPACITOR,FXD,CER,0.05pF	230-35	R23	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C14	CAPACITOR,FXD,CER,0.05pF	230-35	R24	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C15	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R25	RESISTOR,FXD,MF,2K,1%,0.25W	110-2K-1
C16	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R26	RESISTOR,FXD,MF,100,1%,0.25W	110-100-1
C17	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R27	RESISTOR,FXD,MF,205,1%,0.25W	110-205-1
C18	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R28	RESISTOR,FXD,MF,100,1%,0.25W	110-100-1
C19	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R29	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
C20	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R30	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C21	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R31	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C22	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R32	RESISTOR,FXD,MF,61.9,1%,0.25W	110-61.9-1
C23	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R33	RESISTOR,FXD,MF,61.9,1%,0.25W	110-61.9-1
C24	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R34	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C25	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R37	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C26	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R38	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1
C27	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R39	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1
C28	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R40	RESISTOR,FXD,MF,14.7K,1%,0.25W	110-14.7K-1
C29	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R41	RESISTOR,FXD,MF,14.7K,1%,0.25W	110-14.7K-1
C30	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	R42	RESISTOR,FXD,MF,110,1%,0.25W	110-110-1
C31	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U1	IC,MICROPROCESSOR	54-448
C32	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U2	IC,TTL,74LS32,QUAD,2 INPUT OR	54-74LS32
C33	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U3	IC,TTL,74LS04,HEX,INVERTERS	54-74LS04
C34	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U4	IC,TTL,74LS266,QUAD,2 INPUT XN	54-74LS266
C35	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U5	IC	54-447
C36	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U6	IC,TTL,74LS74,DUAL,D FLIP FLOP	54-44
C37	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U7	IC,TTL,74LS20,DUAL,4 INPUT NAN	54-74LS20
C38	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U8	IC,TTL,74LS04,HEX,INVERTERS	54-74LS04
C39	CAPACITOR,FXD,TANT,1pF,10%,35V	250-19	U9	IC,TTL,74LS194,4 BIT SHIFT R	54-122
C41	CAPACITOR,FXD,MICA,150pF	230-150	U10	IC,TTL,74LS00,QUAD,2 INPUT NAN	54-74LS00
C43	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U11	IC,TTL,74LS74,DUAL,D FLIP FLOP	54-44
C44	CAPACITOR,FXD,CER,0.1pF,20%,10V	230-37	U12	IC,TTL,74LS74,DUAL,D FLIP FLOP	54-44
CR1	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	U13	1C,TTL,74LS09,QUAD,2 INPUT AND	54-96
CR2	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	U14	IC,TTL,74LS139,DUAL,2 TO 4 DEC	54-74LS139
CR3	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	U15	IC,TTL,74LS273,OCTAL,D-TYPE	54-350
CR4	DIODE,VARACTOR,MVAM115,440pF	10-61	U16	IC,TTL,74LS257,QUAD,DATA SELEC	54-446
L1	INDUCTOR,FXD,10UH,10%	310-35	U17	IC,TTL,74LS257,QUAD,DATA SELEC	54-446
Q1	TRANSISTOR,NPN,2N3563,SI,RF-IF	20-2N3563	U18	IC,TTL,74LS166,8 BIT SHIFT	54-396
Q2	TRANSISTOR,NPN,2N3563,SI,RF-IF	20-2N3563	U19	IC,TTL,74LS166,8 BIT SHIFT	54-396
Q3	TRANSISTOR,NPN,2N2218,SI,MED-F	20-2N2218	U20	IC,TTL,74LS245,OCTAL BIDIREC	54-344
Q4	TRANSISTOR,NPN,2N2218,SI,MED-F	20-2N2218	U21	IC,TTL,74LS245,OCTAL BIDIREC	54-344
R1	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1	U22	IC,TTL,74LS166,8 BIT SHIFT	54-396
R2	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1	U23	IC,TTL,74LS166,8 BIT SHIFT	54-396
R3	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1	U24	IC,TTL,74LS245,OCTAL BIDIREC	54-344
R4	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1	U25	IC,TTL,74LS245,OCTAL BIDIREC	54-344
R5	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1	U26	IC,TTL,74LS166,8 BIT SHIFT	54-396
R6	RESISTOR,FXD,MF,750,1%,0.25W	110-750-1	U27	IC,TTL,74LS166,8 BIT SHIFT	54-396
R7	RESISTOR,FXD,MF,750,1%,0.25W	110-750-1	U28	IC,TTL,74LS245,OCTAL BIDIREC	54-344
R9	RESISTOR,TRIM,CER,2K,10%,1T	156-2K	U29	IC,TTL,74LS245,OCTAL BIDIREC	54-344
R10	RESISTOR,TRIM,CER,2K,10%,1T	156-2K	U30	IC,MEMORY,TMS4416-15NL,DRAM	54-378
R11	RESISTOR,FXD,MF,750,1%,0.25W	110-750-1	U31	IC,MEMORY,TMS4416-15NL,DRAM	54-378
R11	RESISTOR,TRIM,CER,2K,10%,1T	156-2K	U32	IC,MEMORY,TMS4416-15NL,DRAM	54-378
R12	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1	U33	IC,MEMORY,TMS4416-15NL,DRAM	54-378
R13	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1	U34	IC,MEMORY,TMS4416-15NL,DRAM	54-378
R14	RESISTOR,FXD,MF,21.5,1%,0.25W	110-21.5-1	U35	IC,MEMORY,TMS4416-15NL,DRAM	54-378

Table 7-9. A7 GDP PCB (D30004-3) Continued

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
U36	IC,MEMORY,TMS4416-15NL,DRAM	54-378	U41	IC,MEMORY,TMS4416-15NL,DRAM	54-378
U37	IC,MEMORY,TMS4416-15NL,DRAM	54-378	U42	IC,TTL,74LS367,HEX,BUS DRIVERS	74LS367
U38	IC,MEMORY,TMS4416-15NL,DRAM	54-378	U43	IC,TTL,74LS132,QUAD,NAND SCHMIDT	54-74LS132
U39	IC,MEMORY,TMS4416-15NL,DRAM	54-378			
U40	IC,MEMORY,TMS4416-15NL,DRAM	54-378			

Table 7-10. A9 PCB (D30007-3)

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
C1	CAPACITOR,FIXED,ALUM POLAR	250-139	CR11	DIODE,RECTIFIER,IN4003,200V	10-SI2
C2	CAPACITOR,FXD,TANT,6.8µF,10%,3V	250-41	CR12	DIODE,RECTIFIER,IN4003,200V	10-SI2
C3	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	CR13	DIODE,RECTIFIER,IN4003,200V	10-SI2
C4	CAPACITOR,FIXED,ALUM,POLAR	250-138	CR14	DIODE,RECTIFIER,IN4003,200V	10-SI2
C5	CAPACITOR,FXD,TANT,6.8µF,10%,3V	250-41	CR15	DIODE,RECTIFIER,IN4003,200V	10-SI2
C6	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	CR17	DIODE,RECTIFIER,IN4003,200V	10-SI2
C7	CAPACITOR,FIXED,ALUM POLAR	250-140	CR19	DIODE,RECTIFIER,IN4003,200V	10-SI2
C8	CAPACITOR,FXD,TANT,6.8µF,10%,3V	250-41	CR20	DIODE,RECTIFIER,IN4003,200V	10-SI2
C9	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	CR21	DIODE,RECTIFIER,IN4003,200V	10-SI2
C10	CAPACITOR,FIXED,ALUM POLAR	250-137	CR22	DIODE,RECTIFIER,IN4003,200V	10-SI2
C11	CAPACITOR,FXD,TANT,6.8µF,10%,3V	250-41	CR23	DIODE,RECTIFIER,IN4003,200V	10-SI2
C12	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	DS1	INDICATOR,LED,YEL,PANEL	15-32
C13	CAPACITOR,FIXED,ALUM POLAR	250-137	F1	FUSE,7A	631-53
C14	CAPACITOR,FXD,TANT,6.8µF,10%,3V	250-41	P1	CONNECTOR,HEADER,1 ROW-0.156	551-575
C15	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	P2	CONNECTOR,HEADER,1 ROW-0.1	551-573
C16	CAPACITOR,FIXED,ALUM POLAR	250-140	P3	CONNECTOR,HEADER,1 ROW-0.156	551-576
C17	CAPACITOR,FXD,TANT,6.8µF,10%,3V	250-41	P4	CONNECTOR,HEADER,1 ROW-0.156	551-574
C18	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R1	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
C19	CAPACITOR,FIXED,ALUM POLAR	250-140	R2	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
C20	CAPACITOR,FXD,TANT,6.8µF,10%,3V	250-41	R3	RESISTOR,FXD,MF,287,1%,0.25W	110-287-1
C21	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R4	RESISTOR,FXD,MF,20.5K,1%,0.25W	110-20.5K-1
C22	CAPACITOR,FIXED,ALUM POLAR	250-137	R5	RESISTOR,FXD,MF,20.5K,1%,0.25W	110-20.5K-1
C23	CAPACITOR,FXD,TANT,6.8µF,10%,3V	250-41	R6	RESISTOR,FXD,MF,20.5K,1%,0.25W	110-20.5K-1
C24	CAPACITOR,FXD,TANT,6.8µF,10%,3V	250-41	R7	RESISTOR,FXD,MF,20.5K,1%,0.25W	110-20.5K-1
C25	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R8	RESISTOR,FXD,MF,20.5K,1%,0.25W	110-20.5K-1
C26	CAPACITOR,FXD,PEST,0.047µF,10%	210-28	R9	RESISTOR,FXD,MF,10.5K,1%,0.25W	110-10.5K-1
CR1	DIODE,RECTIFIER,S02,200V	10-62	R10	RESISTOR,FXD,MF,20.5K,1%,0.25W	110-20.5K-1
CR2	DIODE,RECTIFIER,IN4003,200V	10-SI2	R11	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
CR3	DIODE,RECTIFIER,IN4003,200V	10-SI2	R12	RESISTOR,FXD,MF,20.5K,1%,0.25W	110-20.5K-1
CR4	DIODE,RECTIFIER,IN4003,200V	10-SI2	U1	IC,VOLTAGE REGULATOR,LM340	54-LM340T
CR5	DIODE,RECTIFIER,IN4003,200V	10-SI2	U3	IC,VOLTAGE REGULATOR,7918,-18V	54-63
CR6	DIODE,RECTIFIER,S02,200V	10-62	U4	IC,VOLTAGE REGULATOR,7815,15V	54-MC7815CP
CR7	DIODE,RECTIFIER,S02,200V	10-62	U5	IC,VOLTAGE REGULATOR,7915,-15V	54-MC7915CP
CR8	DIODE,RECTIFIER,S02,200V	10-62	U6	IC,VOLTAGE REGULATOR,7818,18V	54-62
CR9	DIODE,RECTIFIER,IN4003,200V	10-SI2	U7	IC,VOLTAGE REGULATOR,7918,-18V	54-63
CR10	DIODE,RECTIFIER,IN4003,200V	10-SI2	U8	IC,VOLTAGE REGULATOR,7815,15V	54-MC7815CP

Table 7-11. A2 5V Regulator Assembly (C30041-3)

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
C1	CAP, FXD, CER, 0.1UF, 20%, 10%	230-37	R1	RES, FXD, MF, 750, 1% 0.25%	110-750-1
C2	CAP, FXD, TANT, 10UF, 10%, 25V	250-42	R2	RES, FXD,MF, 237, 1%, 0.25%	110-237-1
C3	CAP, FXD, TANT, 1UF, 10%, 35V	250-19A	—	CABLE A9P4 TO A2P1	B30047
CR2	DIODE, RECT, IN4003, 200V	10-S12	U1	IC VOLT REG LM338	54-573
CR3	DIODE, RECT, IN4003, 200V	10-S12			

Table 7-12. A10 Motherboard PCB (D30008-3)

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
C1	CAPACITOR,FXD,CER,0.05µF	230-35	P7	CONNECTOR,HEADER,1 ROW 0.1	551-567
C2	CAPACITOR,FXD,CER,0.05µF	230-35	P8	CONNECTOR,EDGE CARD,PNL MNT,56	551-198
C3	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	P9	CONNECTOR,EDGE CARD,PNL MNT,56	551-198
C4	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	Q1	TRANSISTOR,NPN,2N3694,SI,GEN P	20-2N3694
C5	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R1	RESISTOR,FXD,MF,1K,1%,0.25W	110-1K-1
C6	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R2	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
C7	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R3	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
C8	CAPACITOR,FXD,CER,0.1µF,20%,10V	230-37	R4	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
P1	CONNECTOR,HEADER,2 ROW-0.1	551-564	R5	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
P2	CONNECTOR,HEADER,2ROW-0.1	551-534	R6	RESISTOR,FXD,MF,10K,1%,0.25W	110-10K-1
P3	CONNECTOR,HEADER,1 ROW 0.1	551-566	U1	IC,TTL,74LS244,OCTAL,BUFFER	54-143
P4	CONNECTOR,HEADER,2 ROW-0.1	551-570	U2	IC,TTL,74LS374,OCTAL,D FLIP FLOP	54-41
P5	CONNECTOR,HEADER,1 ROW-0.156	551-575	U3	IC,TTL,74LS74,DUAL,D FLIP FLOP	54-44
P6	CONNECTOR,HEADER,1ROW-0.98	551-533	U4	IC,TTL,74LS138,3 TO 8 DECODE	54-74LS138

Table 7-13. A11 Auxiliary Control Panel PCB (D30131-3)

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
CR1	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	R2	RESISTOR,FXD,MF,100,1%,0.25W	110-100-1
CR2	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	S1	SWITCH,PUSHBUTTON	430-131
CR3	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	S2	SWITCH,PUSHBUTTON	430-131
CR4	DIODE,SWITCHING,1N4446,75V,4NS	10-1N4446	S3	SWITCH,PUSHBUTTON	430-131
P1	CONNECTOR,HEADER	551-567	S4	SWITCH,PUSHBUTTON	430-131
R1	RESISTOR,VARIABLE,CER,100 OHM	146-7			

Table 7-14. RF Deck

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
1	CABLE ASSY., RF O/P TO FREQ/CONV	B30097	1	MARKER/DOWN CONVERTER ASSY.,6409	C31466
1	SUB-ASSY., YIG/TRANSFORMER	C30098	1	RF OUTPUT ASSY., 50 OHM	B15085
1	4.6 TO 6.6 GHZ OSCILLATOR	C18366	1	RF OUTPUT ASSY., 75 OHM	B15815
1	MARKER/DOWN CONVERTER ASSY.,6407	C31465	1	CABLE ASSY FREQ/CONV TO YIG OSC	B30101

Table 7-15. Options and Accessories

REF DES	DESCRIPTION	WILTRON PART NO.	REF DES	DESCRIPTION	WILTRON PART NO.
	OPTION 1, RACK MOUNT			**OPTION 5, PRINTER AND INTERFACE CABLE**	
	LEFT-SIDED ASSEMBLY	D31425		INKJET PRINTER	2225C
	RIGHT-SIDED ASSEMBLY	D31428		INTERFACE CABLE	2225-1
	OPTION 2, STEP ATTENUATOR			**OPTION 6, PROTECTIVE COVER**	
	ATTENUATOR	C30067		FRONT PANEL COVER	SPEC-D-31359-3
	CABLE ASSY., RF O/P TO ATTEN.	B30095			
	CABLE ASSY. ATTEN TO FREQ/CONV	B30096		**ACCESSORIES**	
				REPLACEMENT INKJET CARTRIDGES (2 EACH)	2225-2
	OPTION 3, GPIB INTERFACE ASSY			FAN FOLD INKJET PRINTER PAPER (2500 SHEETS)	2225-3
	GPIB INTERFACE ASSY	C30039			
	OPTION 4, 75 OHM OUTPUT (6407 ONLY)				
	75 OHM OUTPUT IMPEDANCE	6407/4			

SECTION VIII
SERVICE

Table 8-1. Service Section Organization

SECTION VIII
SERVICE

8-1 INTRODUCTION

This section contains general information, disassembly/reassembly instructions, and service information -- circuit descriptions, schematics, parts locator diagrams, and troubleshooting data --for the overall RF analyzer and individual printed circuit boards (PCBs). This service information is organized as shown in Table 8-1 (facing page).

8-2 GENERAL INFORMATION

8-2.1 Printed Circuit Board (PCB) and Subassembly Exchange Program

WILTRON has an exchange program that includes the assemblies shown in Table 8-2. Upon request, WILTRON will immediately ship a replacement for any RF analyzer PCB or assembly covered by this program. The customer has 30 days in which to return the defective part. Contact Customer Service at 408-778-2000 to make arrangements for an exchange.

8-2.2 Recommended Test Equipment for Troubleshooting

A list of recommended test equipment for troubleshooting the RF analyzer is provided in Table 8-3.

8-2.3 Preventive Maintenance

The air filter on the RF analyzer rear panel should be periodically checked and cleaned as necessary. To gain access, remove the four thumbscrews and the fan guard.

Table 8-2. Exchangeable Subassemblies

SUBASSEMBLY	PART NO.
Control Panel PCB Assembly (A1)	D30040-3
Signal Channel PCB Assembly (A3)	D30002-3
4.4-6.6 GHz Oscillator Assembly	C18366
Down Converter, 1 GHz	C31465
Down Converter, 2 GHz	C31466
RF Output Assembly, 50Ω	B15085
RF Output Assembly, 75Ω	B15815
YIG and ALC PCB Assembly (A4)	D30003-3
Central Processor Unit PCB Assembly (A6)	D30005-3
Graphic Display Processor PCB Assy (A7)	D30004-3
GPIB Option 3 (A8)	C30039
Programmable Attenuator Assembly	C30067
Encoder Control Assembly	B30092
Monitor Assembly	2000-150

Table 8-3. Recommended Test Equipment for Troubleshooting

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED MANUFACTURER
Digital Multimeter	DC Voltage: 0.05% to 30V 0.002% to 10V	John Fluke Co. Model 8600A
Oscilloscope	60 MHz bandwidth, 1mV vertical sensitivity, and variable external horizontal input capability.	Tektronix Models 5440/5A18/5B10
Spectrum Analyzer	60 dB power range. 10 MHz to 7 GHz range. 50 dB signal-to-noise ratio, .01 to 2 GHz	HP 8565A or Tektronix 492
Frequency Counter	10 MHz to 7 GHz range.	HP 5350A or EIP 545A

8-2.4 Static Handling Procedures

This instrument contains electronic components that are subject to being damaged by static electricity. Table 8-4 provides a list of precautions that, if followed, will minimize the possibility of static-shock damages.

8-2.5 Soldering

Xersin solder has been used in selected locations on the rear panel connectors, line module, and power switch. The flux in this solder is non-corrosive and improves the reliability of the connection. Consequently, do not remove residue flux from any solder joint.

8-3 SERVICE INSTRUCTIONS

The service instructions in the following paragraphs contain all of the necessary information--e.g., circuit descriptions, schematics, block diagrams, parts locator diagrams, flow charts--to permit troubleshooting to the defective integrated or functional circuit.

8-4 MICROWAVE COMPONENTS

The microwave components consist of the 6400-6 Series SWR Autotesters and the 6400-71 Series RF Detectors. Functional descriptions of these components, along with instructions for replacing the detector diode in the RF detector and the SWR autotester are provided in the following paragraphs. General information pertaining to care and cleaning of installed RF connectors is also included.

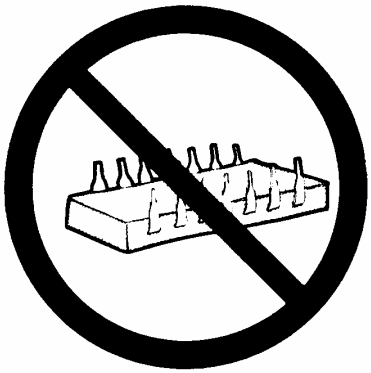
8-4.1 SWR Autotesters

The 6400-6 Series SWR Autotesters are highly accurate devices for making reflection measurements. The components consist of a broadband microwave bridge, a precision termination, a zero-bias Schottky diode, and a low-reflection test port connector. The SWR Autotesters are precision manufactured microwave components. There are no internal adjustments, and repair is limited to diode replacement (paragraph 8-4.3).

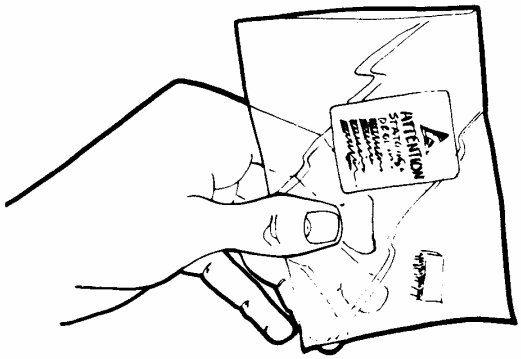
Table 8-4. Static Warning Precautions

1. Do not touch exposed contacts on any static sensitive component.

3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.



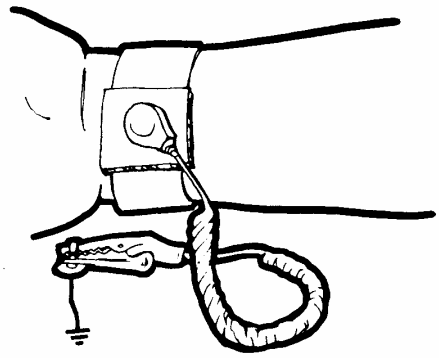
2. Do not slide static sensitive components across any surface.



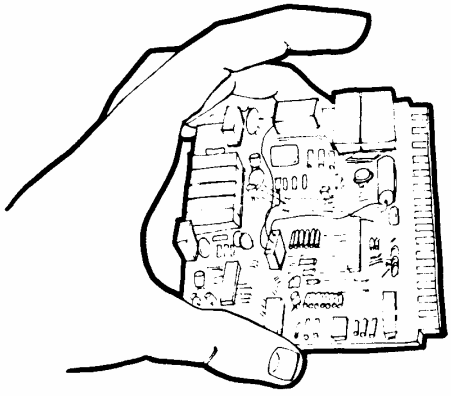
4. Transport and store PCBs and other static sensitive devices in static-shielded containers.

Table 8-4. Static Warning Precautions (Continued)

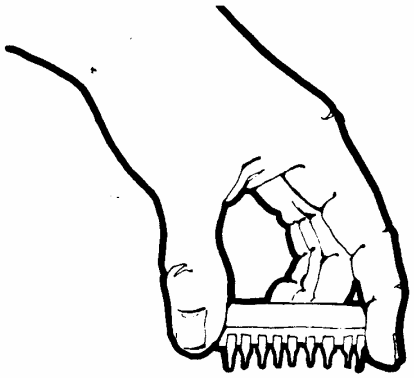
5. Label all static sensitive devices.



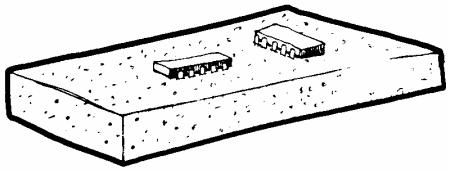
6. Wear a static-discharge wrist-band when working around static sensitive components.



7. Handle PCBs only by their edges.



8. Pick up solid state devices by their bodies and never by their leads.



9. Keep component leads shorted together whenever possible.

10. Additional Guidelines:

- Keep work spaces clean and free of any objects capable of holding or storing an electric charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

8-4.2 Model 6400-71 Series RF Detectors

The 6400-71 series RF detectors provide the 6407/6409 with a 1.0 MHz to 2.0 MHz frequency capability. The detectors are manufactured in 50- and 75-ohm types. The 6400-71N50 and 71B50 types offer an input impedance of 50 ohms; the 6400-71N75 and 71B75 types offer an input impedance of 75 ohms. Both detector types offer exceptionally flat transmission and return loss characteristics, and both have field-replaceable zero-bias Schottky detector diodes.

The Model 6400-71 RF Detector is a precision manufactured microwave component. The only repair recommended is replacement of the detector diode (paragraph 8-4.4).

8-4.3 Diode Replacement, 6400-6 Series SWR Autotesters

The 6400 series SWR Autotesters are equipped with a field-replaceable detector diode. To replace this diode, proceed as follows:

a. Remove the two screws from the top cover of the SWR Autotester (the top cover contains the model number), and remove the cover.

b. Unplug and remove the defective diode (Figure 8-1) from the SWR Autotester circuit board.

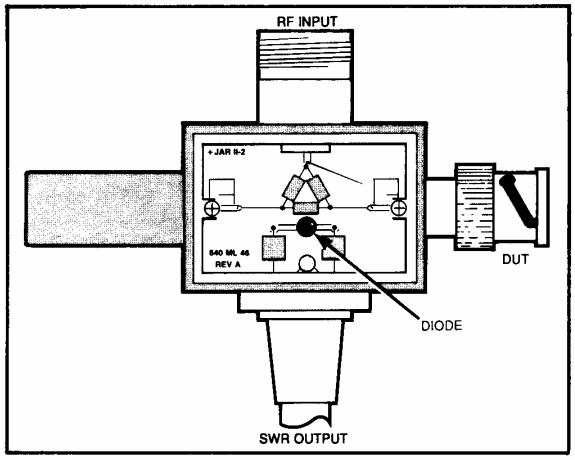


Figure 8-1. Autotester PCB with diode.

c. Install the replacement diode with the white dot (cathode) positioned toward the test port connector (Figure 8-2).

d. If necessary, retune for 40 dB directivity after diode replacement.

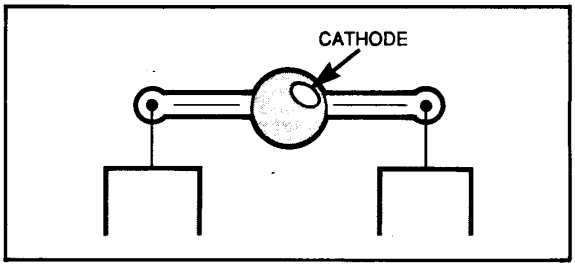


Figure 8-2. Proper Diode orientation.

e. Replace the top cover and reinstall the two screws.

8-4.4 Diode Replacement, 6400-71 Series RF Detectors

The 6400-71 series RF detectors are equipped with a field-replaceable detector diode. Replacement of this diode requires readjustment of two potentiometers located within the detector housing. The readjustment of these potentiometers is accomplished after the defective diode is removed, but before the replacement diode is installed. To set the resistance of these two potentiometers, use a digital multimeter that has a least a 3-1/2 digit display resolution. To replace the diode, proceed as follows:

a. Remove the four retaining screws and lift the top cover away from the detector housing.

b. Unplug the defective diode (Figure 8-3) from the circuit board and remove the diode from the detector.

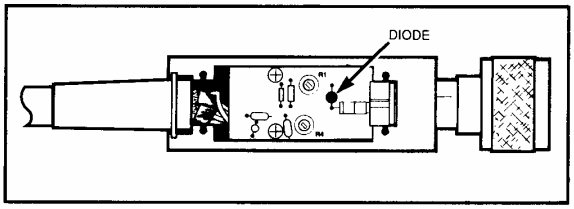


Figure 8-3. Detector PCB

c. Adjust potentiometer R1 fully clockwise (maximum resistance).

d. Connect the digital multimeter between pins 1 and 2 of the detector connector (Figure 8-4).

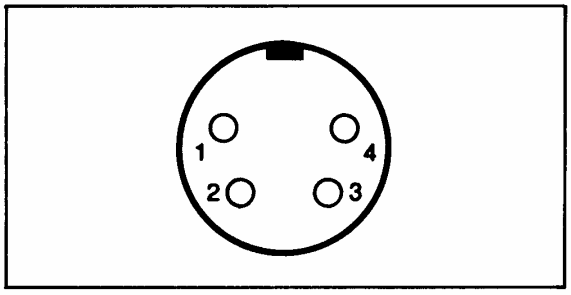


Figure 8-4. Detector PIN orientation.

e. Measure the resistance of R1 (typical value is 40.5 kΩ). This resistance value is hereafter known as R_T; record this value.

f. Obtain the K value from the label (Figure 8-5) on the replacement module's plastic container.

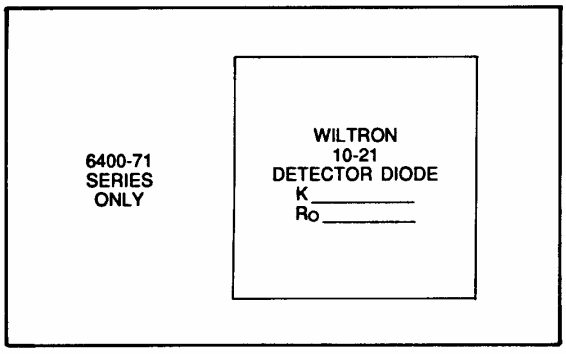


Figure 8-5. Label from replacement module container.

g. Multiply K times R_T (K x R_T) and record the product.

h. Adjust R1 counterclockwise until the digital multimeter indicates the resistance value calculated in step g.

i. Disconnect the multimeter leads from between pins 1 and 2.

j. Connect the multimeter leads between pin 3 and the connector shield.

k. Note the R_O value on the label from the replacement module container (Figure 8-5).

l. Adjust R4 until the multimeter indicates the R_O value.

m. Disconnect the multimeter from the detector.

n. Orient the replacement diode so that the white dot (cathode) is positioned as shown in Figure 8-6.

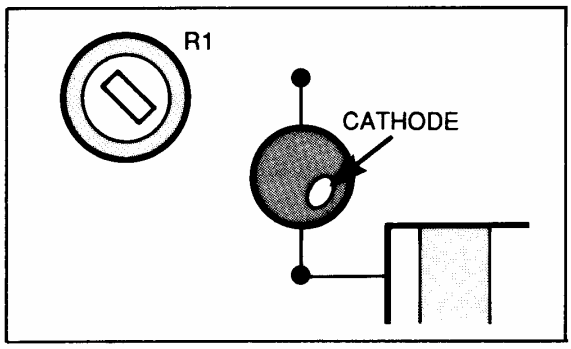


Figure 8-6. Proper diode orientation.

o. Insert the diode into the socket on the A1 PCB.

p. Reinstall the top cover, securing it with the four retaining screws.

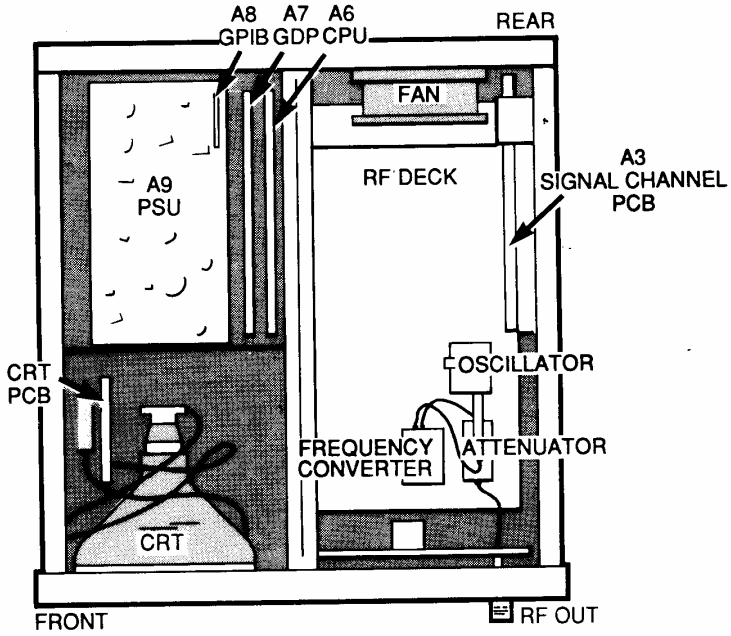
8-4.5 Connector Cleaning

Connector interfaces should be kept clean and free of dirt and other debris. Alcohol and a cotton swab work fine as cleaning agent and applicator.

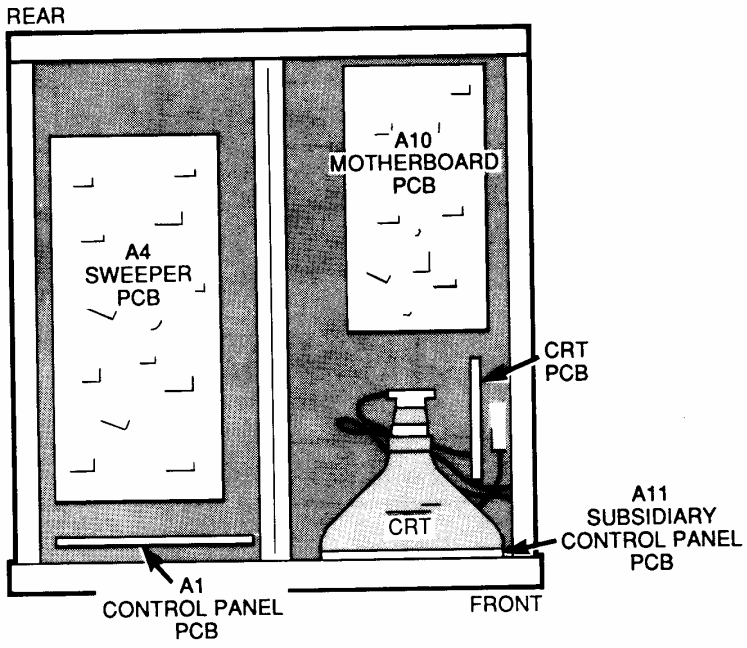
8-5 GAINING ACCESS TO PCBs

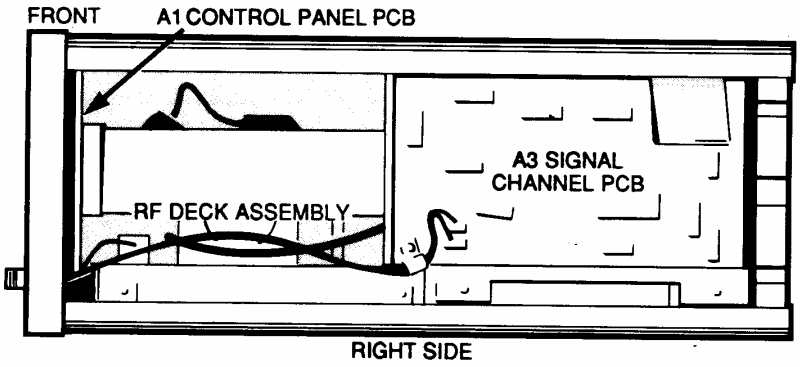
To gain access to the interior of the instrument, remove the four corner brackets on the rear of the 6400 and slide the top, bottom, and side panels to the rear. The illustrations in Figure 8-7 show the 6400 interior with PCBs, RF components deck, and CRT display, adjustments, and driver board.

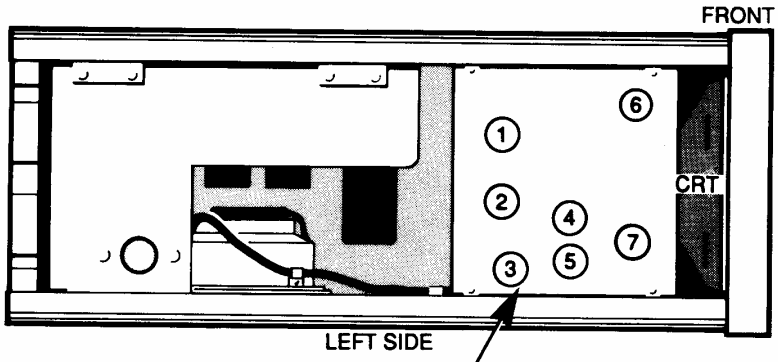
TOP VIEW



BOTTOM VIEW







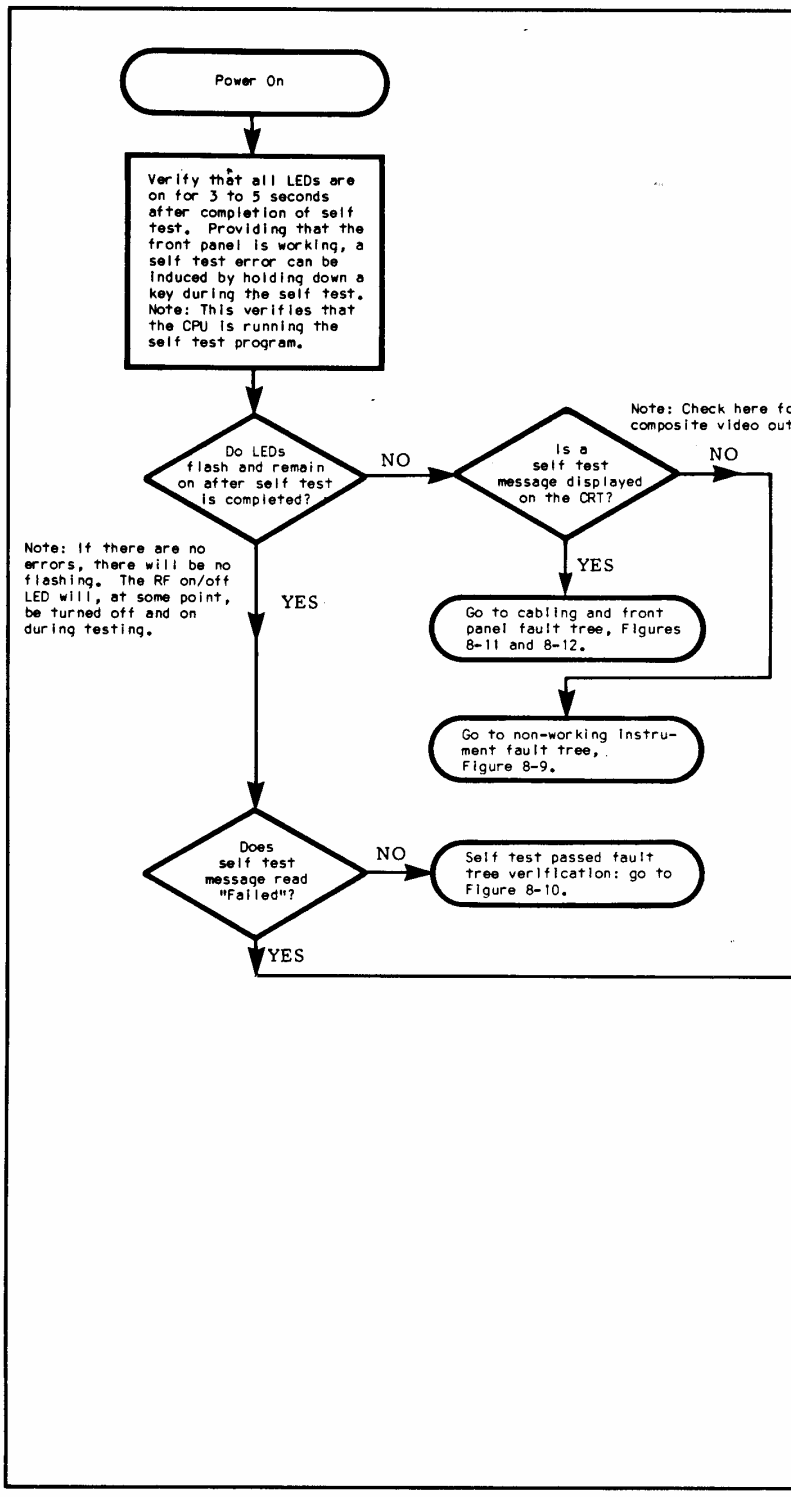
CRT ADJUSTMENTS

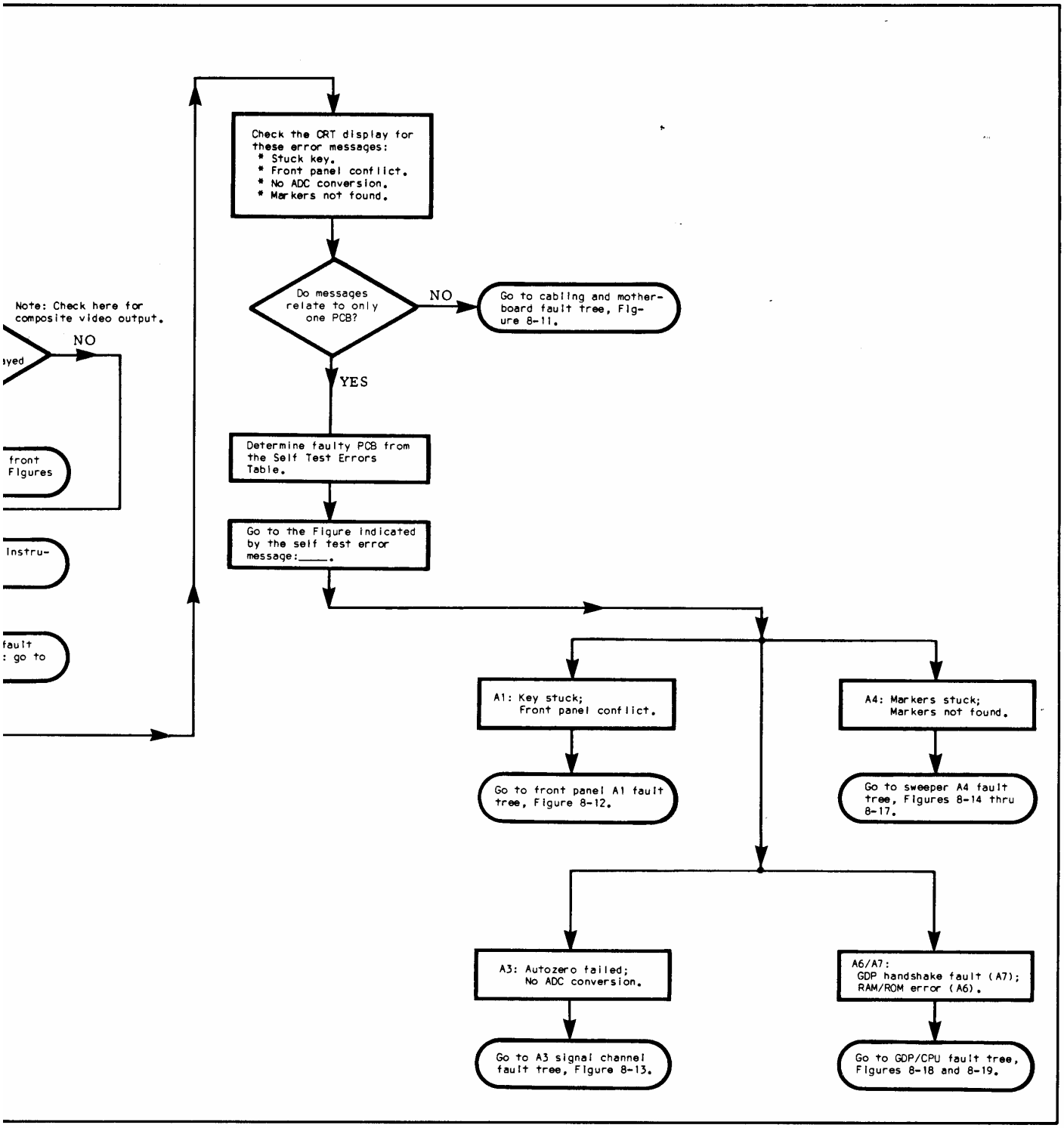
1. Brilliance
2. Horizontal Hold
3. Contrast
4. General Linearization
5. Bottom Linearization
6. Horizontal Amplitude
7. Vertical Amplitude

Figure 8-7. 6400 Interior

8-6 Troubleshooting Flow Charts

Troubleshooting to a PCB assembly is accomplished using front panel controls and, where necessary, logical troubleshooting flow charts. Table 3-5 provides the format for using front panel controls to troubleshoot to a malfunctioning PCB. Where further troubleshooting is necessary, the troubleshooting flow charts in Figures 8-8 thru 8-20 are provided.





Paragraph 8-6

Figure 8-8. Self Test on Operational Instrument With Detector and Autotester Probes Connected.

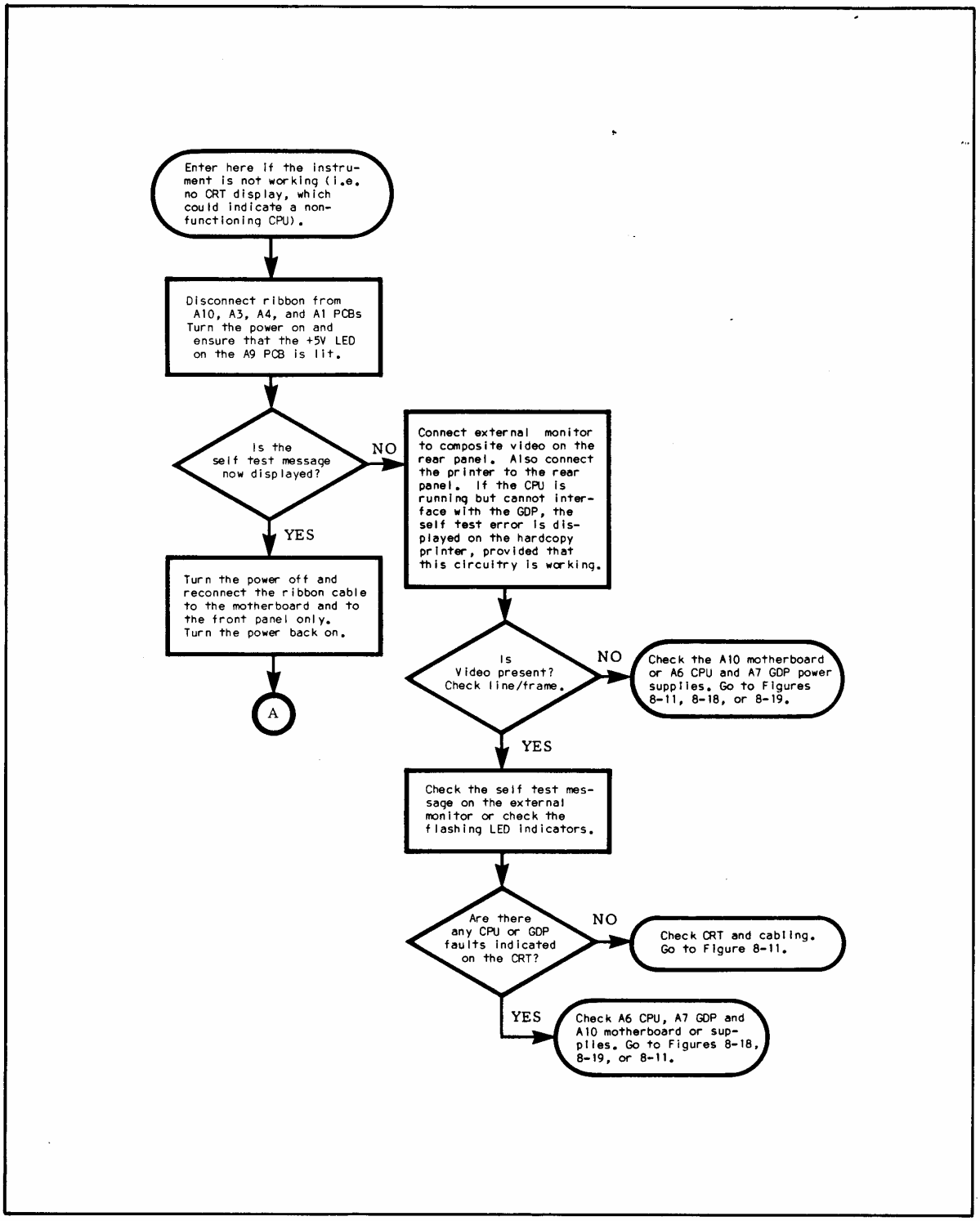


Figure 8-9. Non-Operational Instrument.

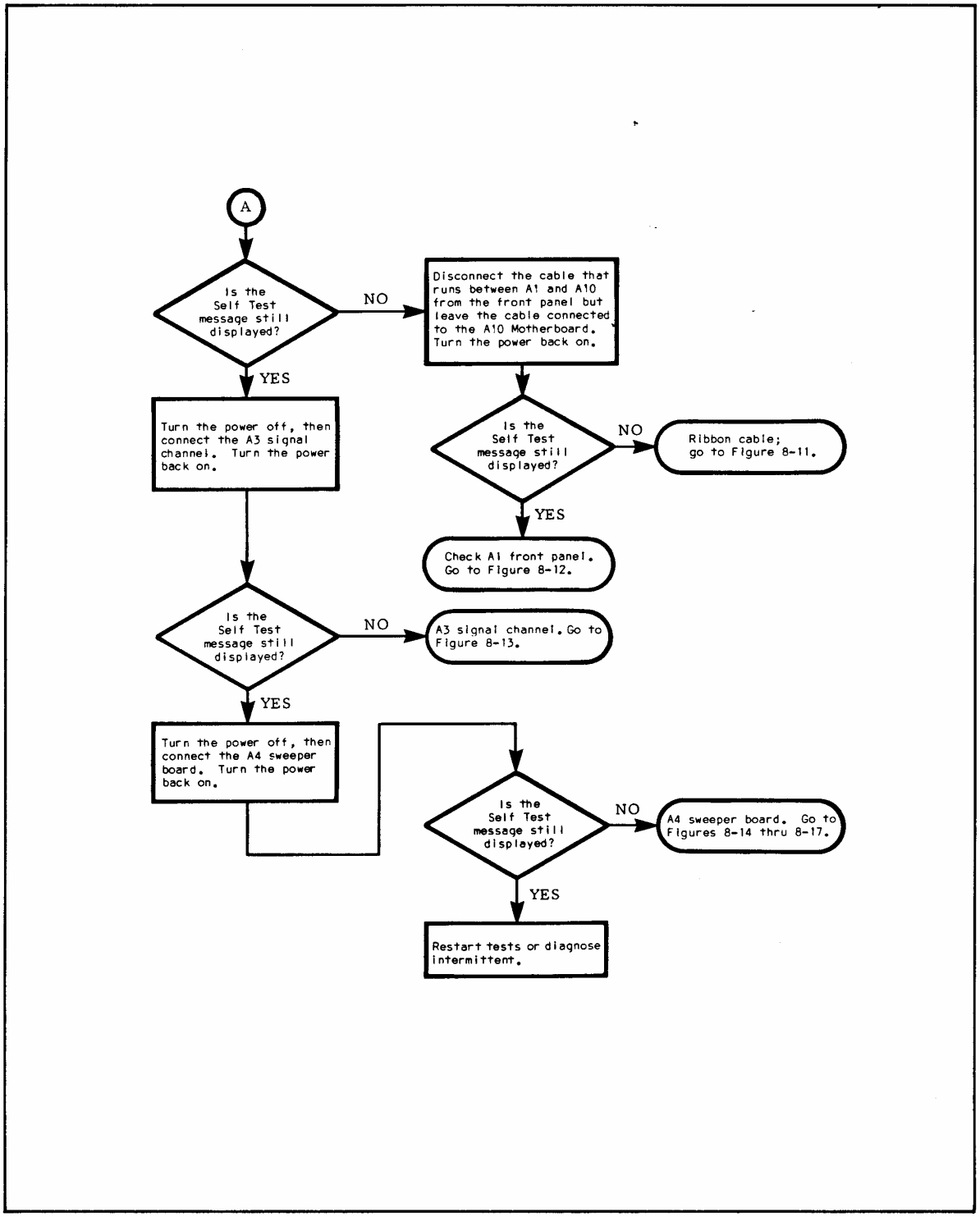


Figure 8-9. Non-Operational Instrument (continued).

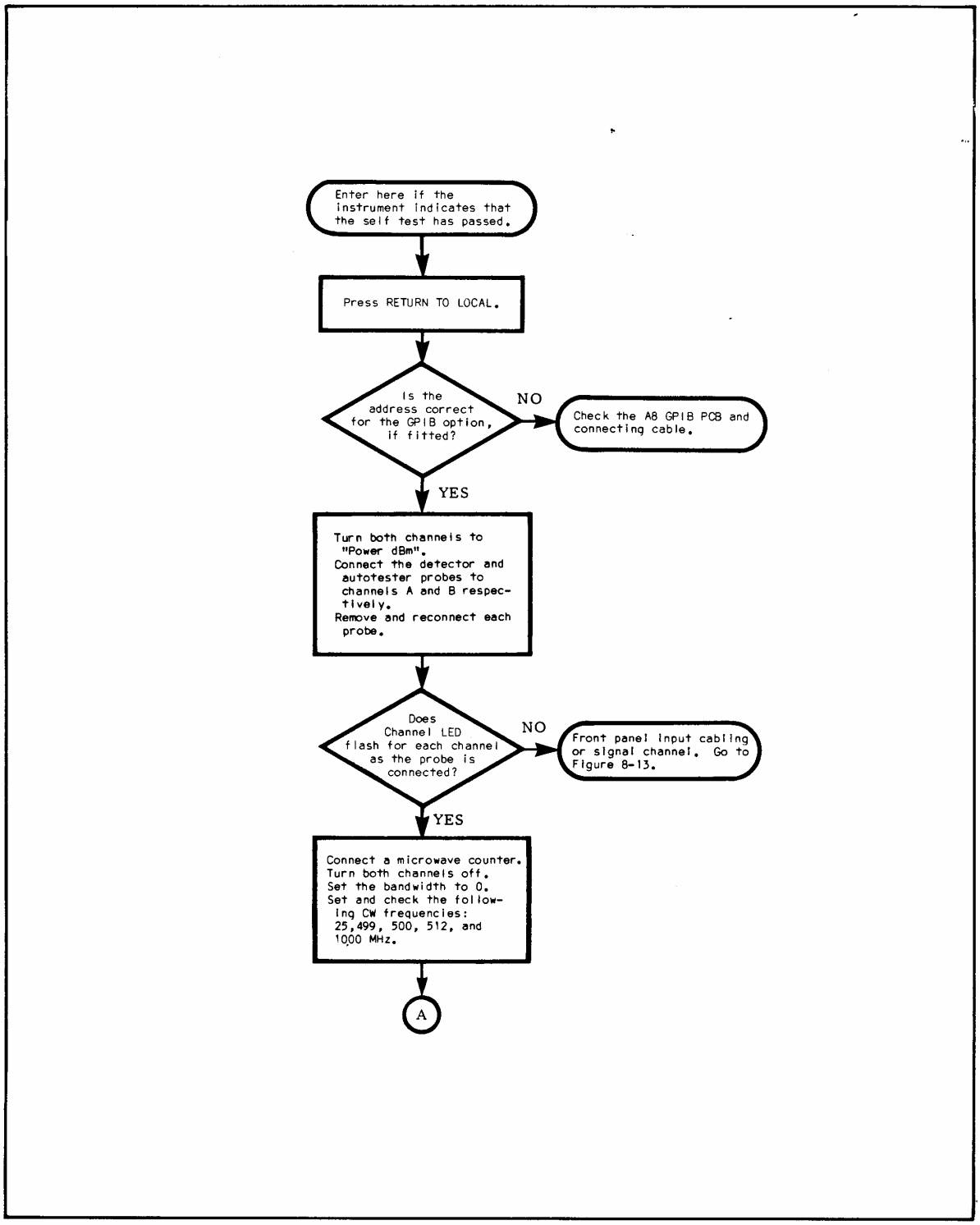


Figure 8-10. Further Diagnostics Following Successful Self Test and Initial Verification.

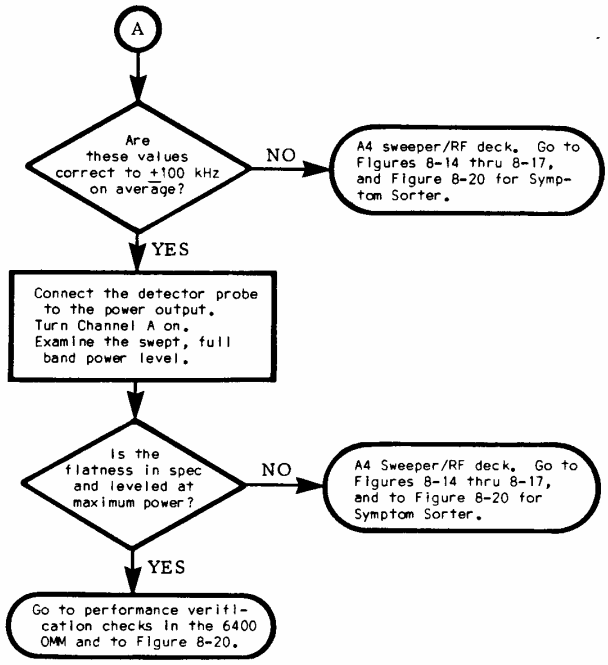


Figure 8-10. Further Diagnostics Following Successful Self Test and Initial Verification (continued).

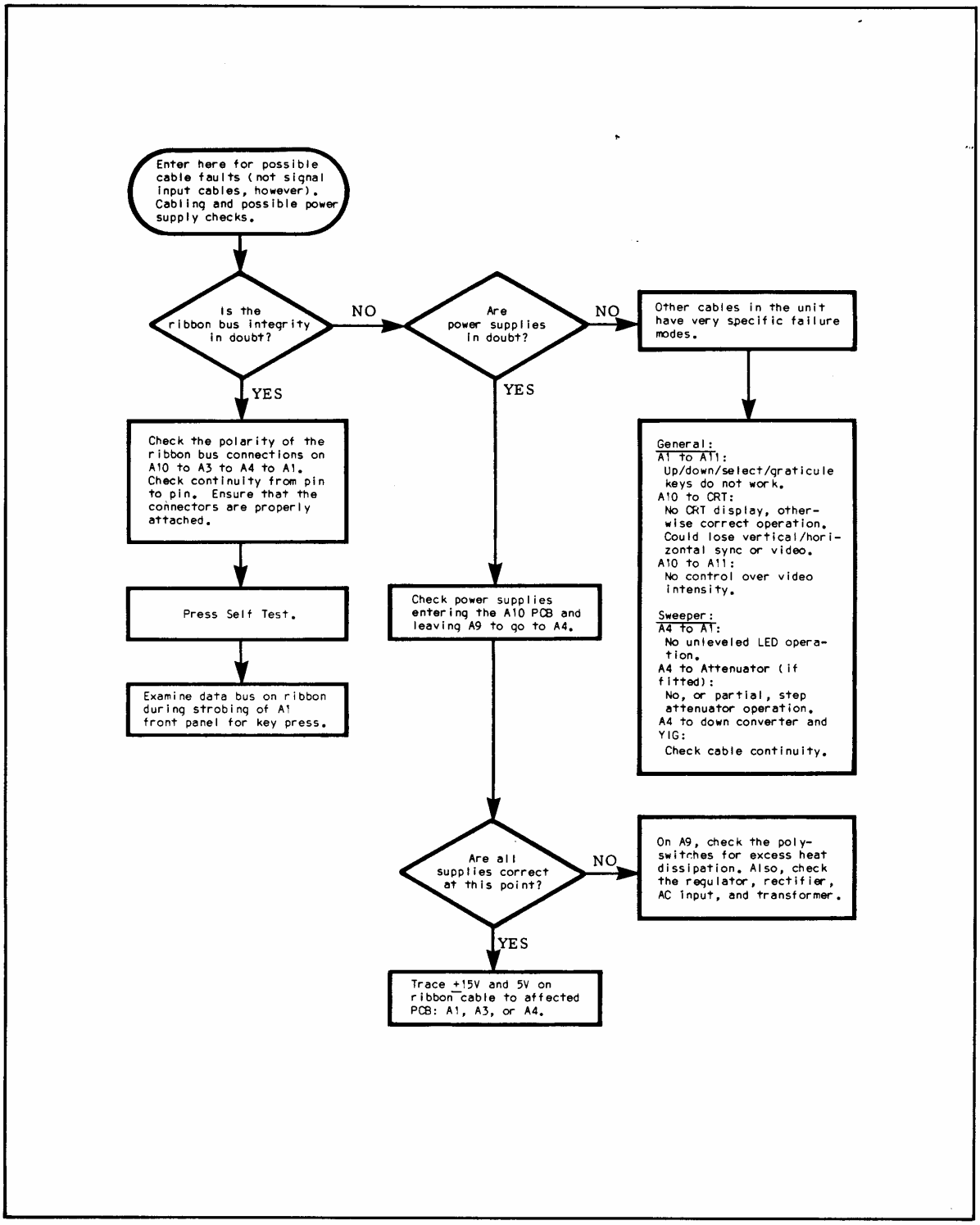


Figure 8-11. Troubleshooting A10 Motherboard and Associated Cabling/A9 Power Supply PCB (continued).

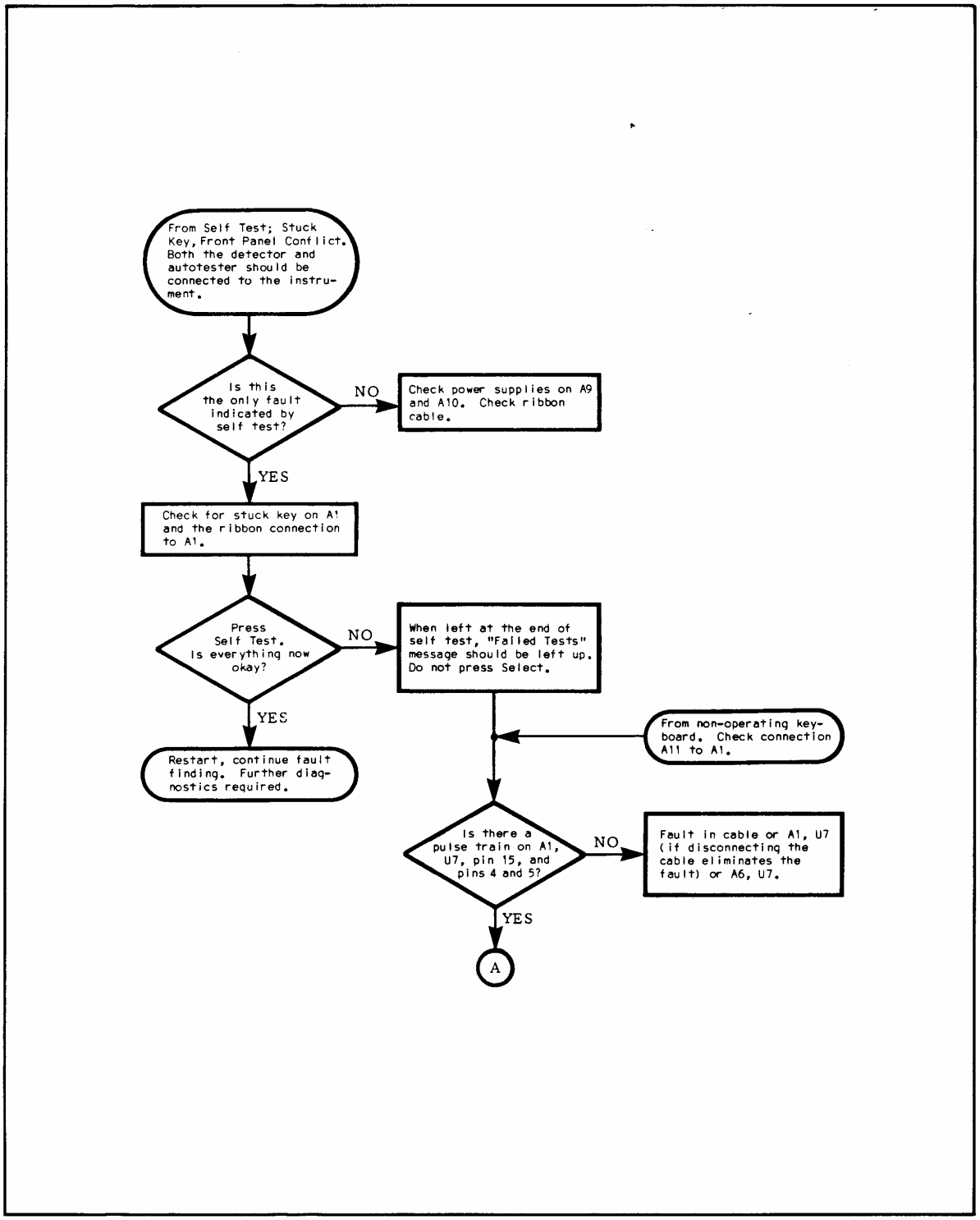


Figure 8-12. A1 PCB Self Test Errors: Stuck Key and Front Panel Conflict.

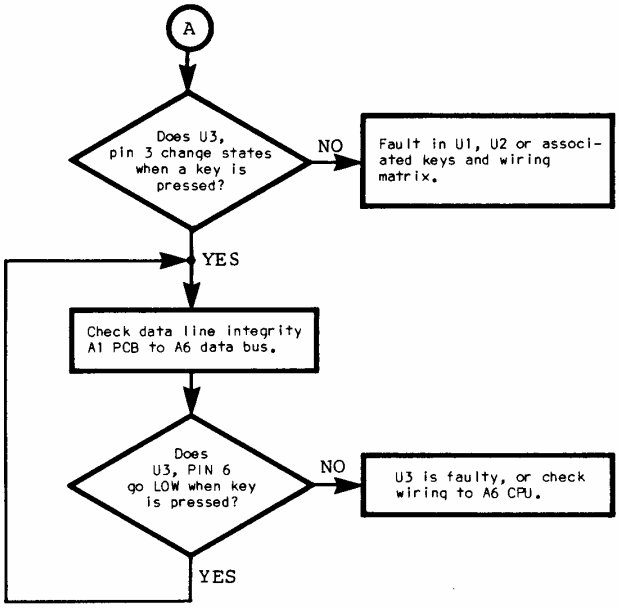


Figure 8-12. A1 PCB Self Test Errors: Stuck Key and Front Panel Conflict (continued).

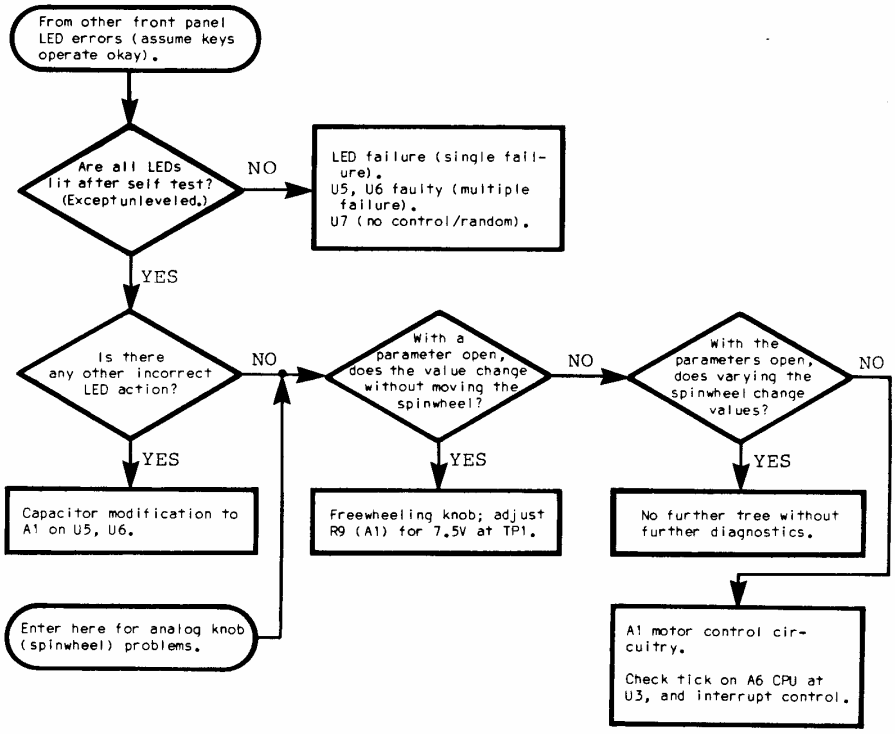


Figure 8-12. A1 PCB Self Test Errors: Stuck Key and Front Panel Conflict (continued).

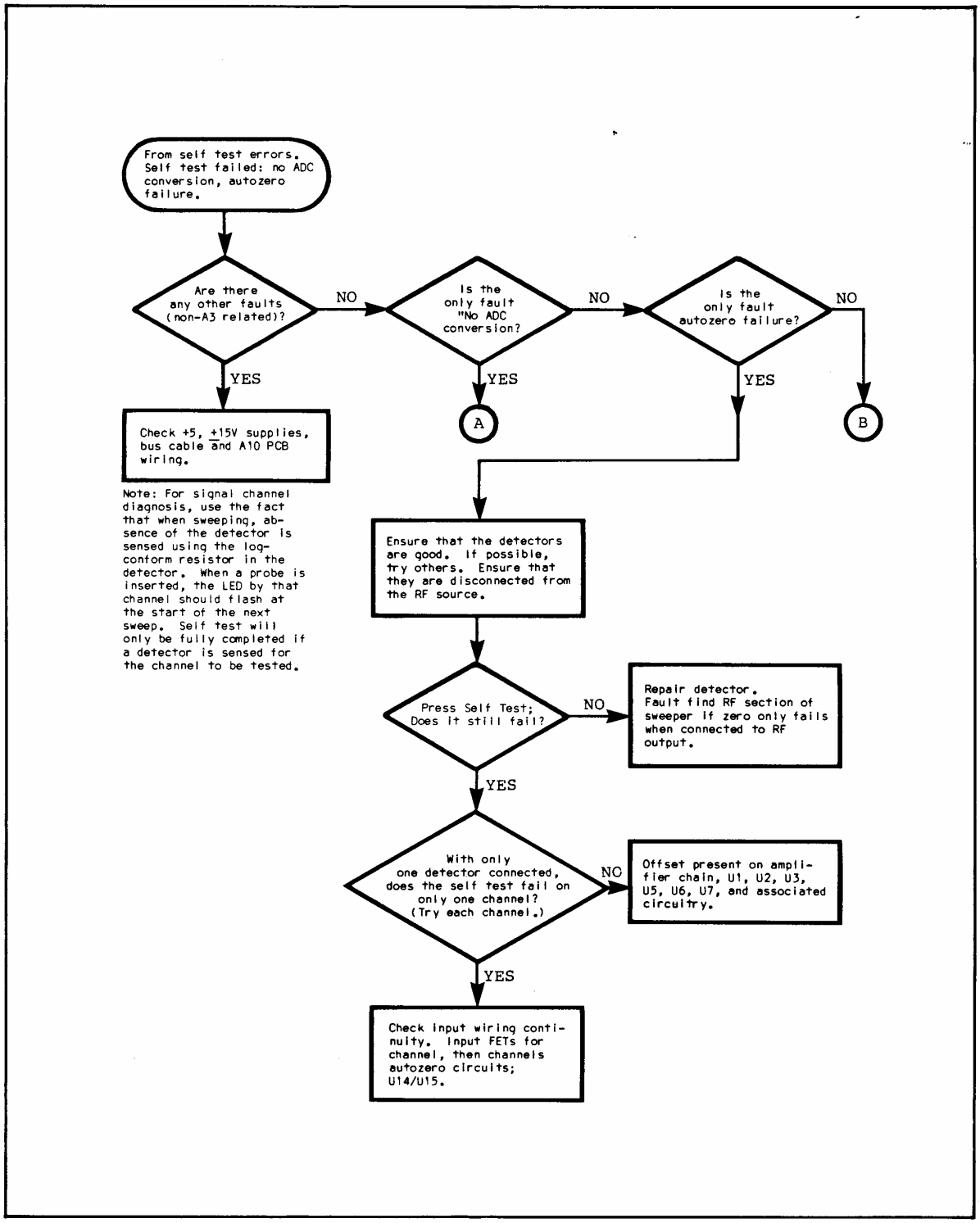


Figure 8-13. Self Test Failed: No ADC Conversion/Autozero Failure.

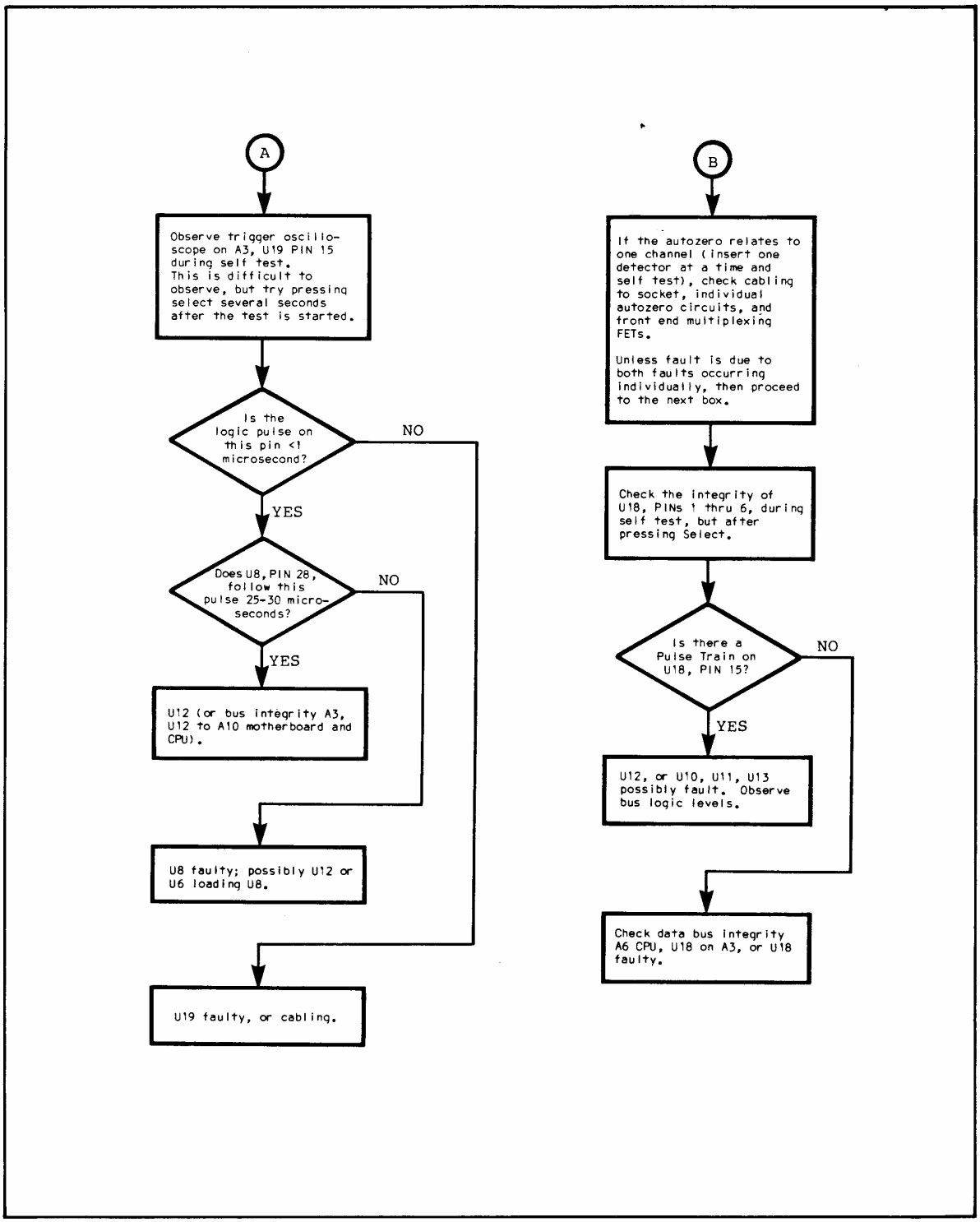


Figure 8-13. Self Test Failed: No ADC Conversion/Autozero Failure (continued).

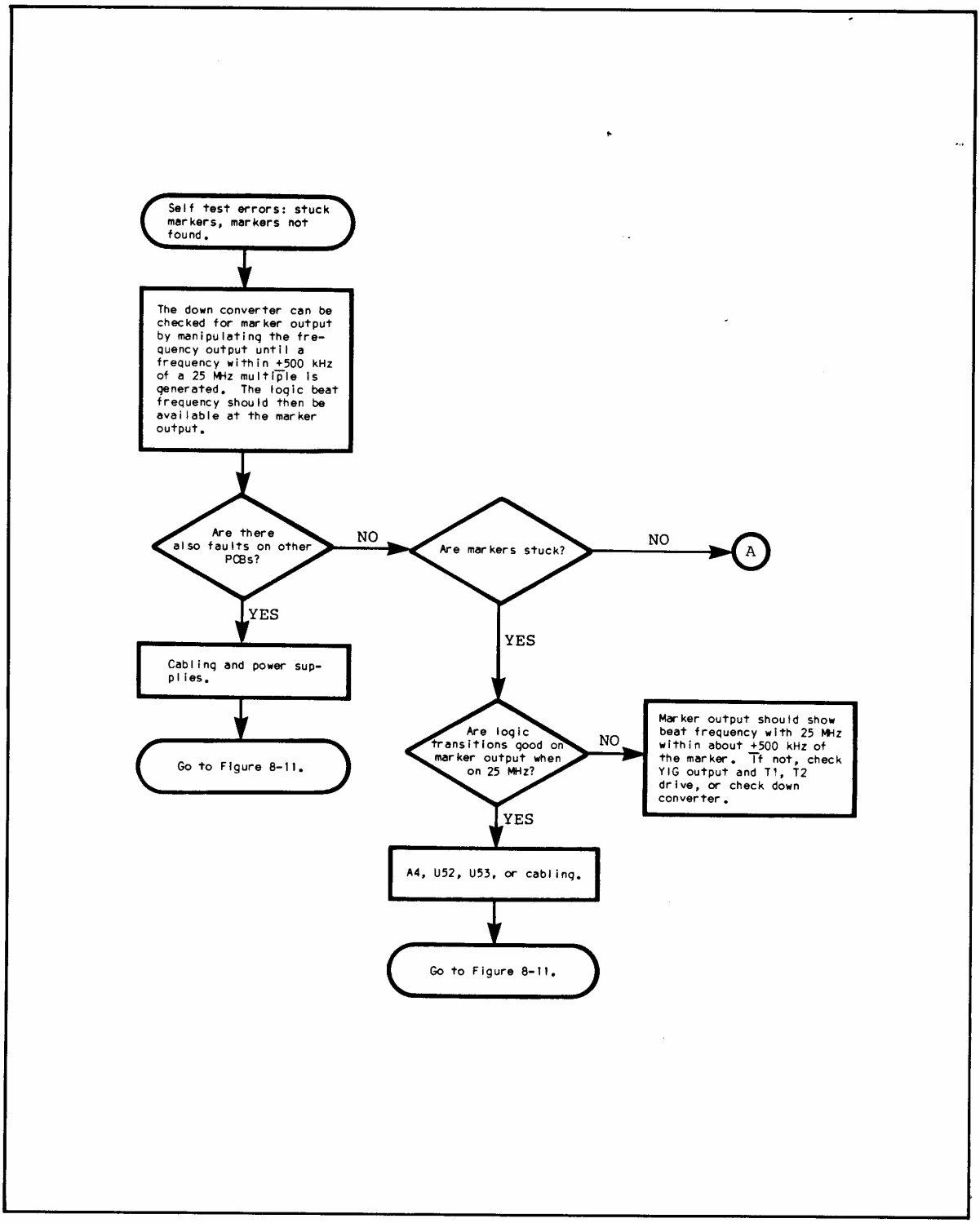


Figure 8-14. Self Test Errors: Stuck Markers/Markers Not Found.

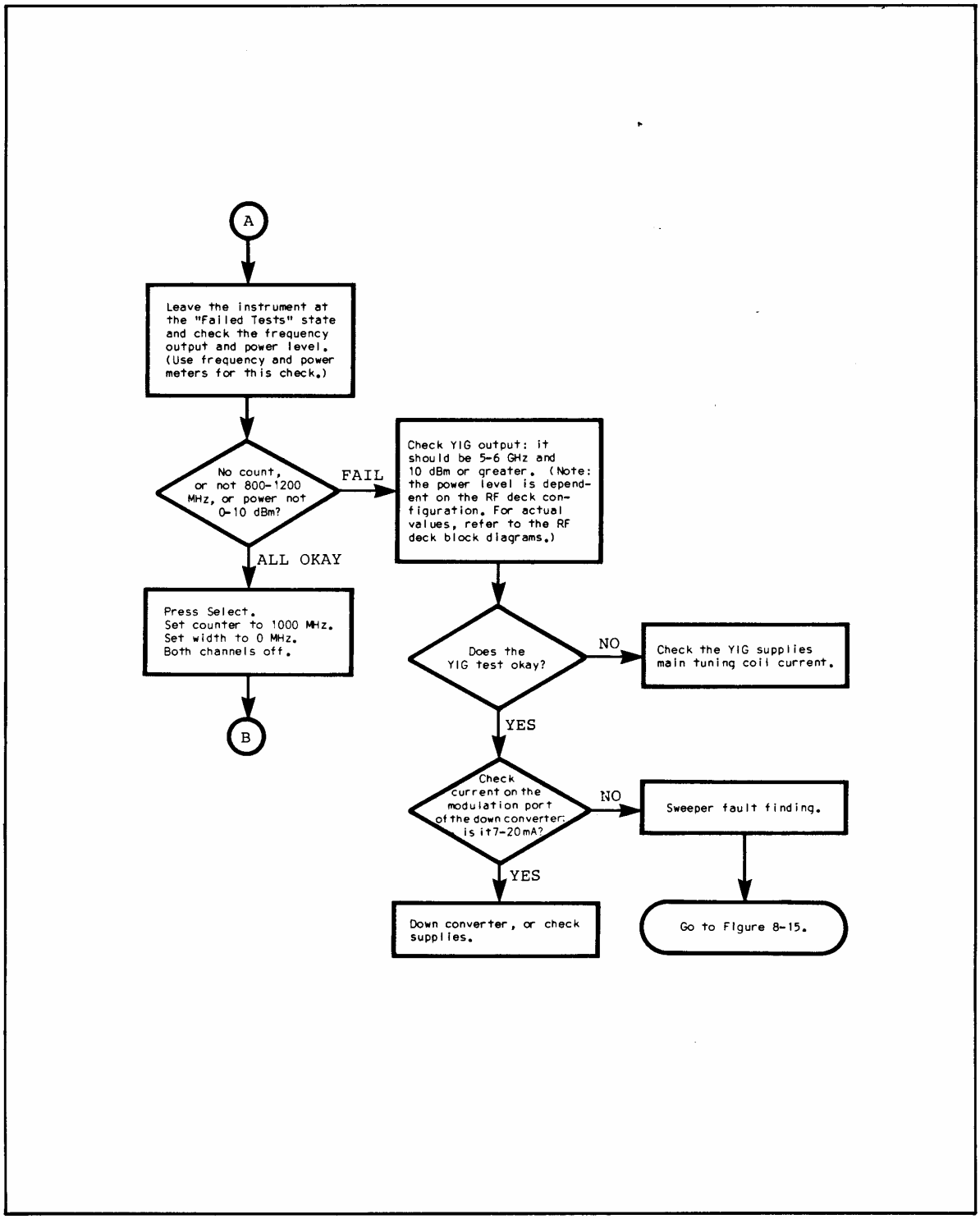


Figure 8-14. Self Test Errors: Stuck Markers/Markers Not Found (continued).

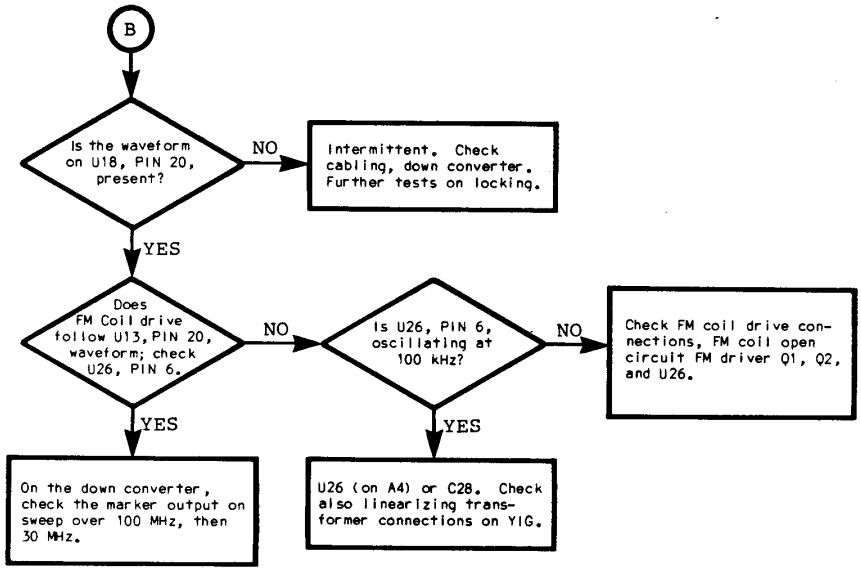


Figure 8-14. Self Test Errors: Stuck Markers/Markers Not Found (continued).

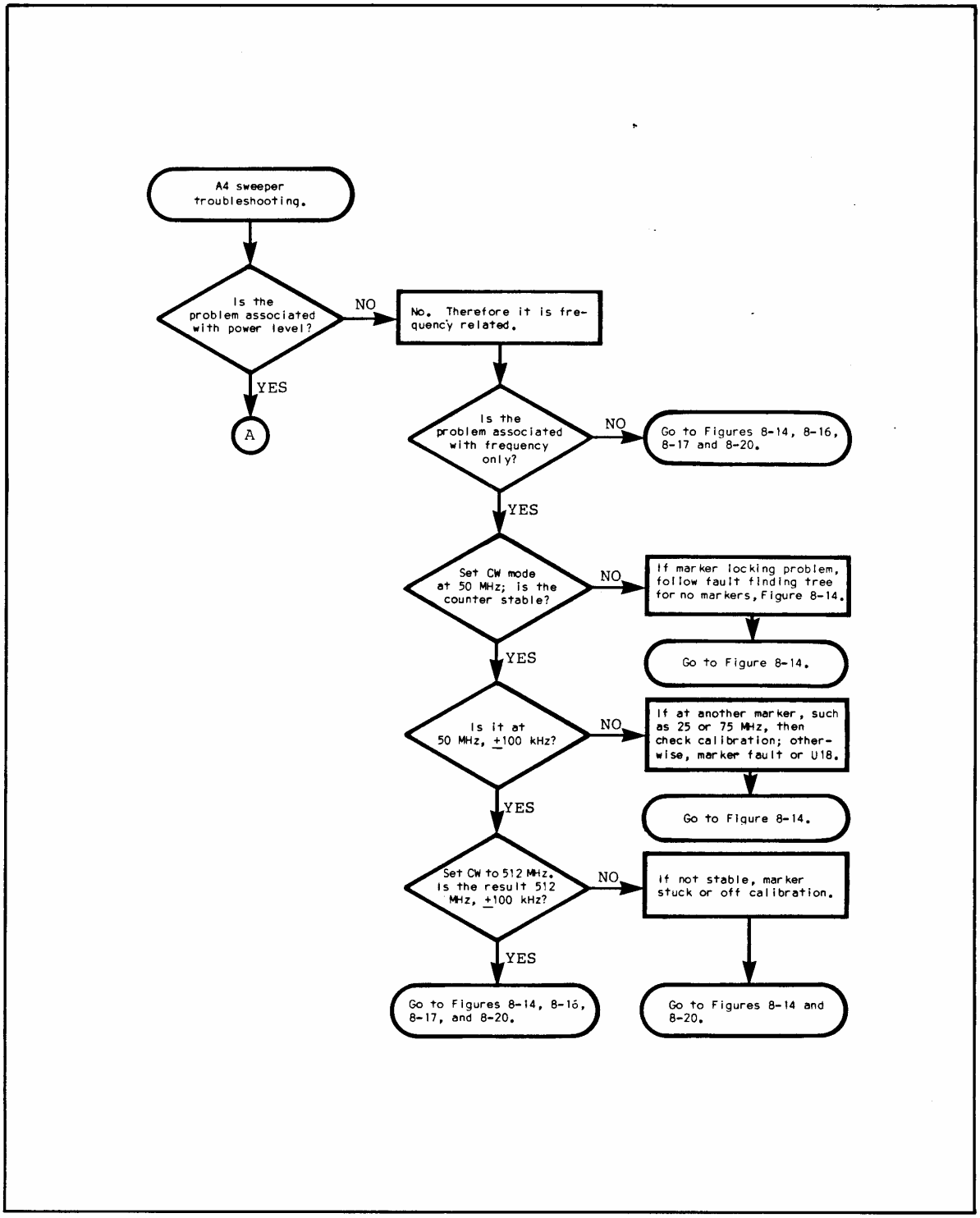


Figure 8-15. Troubleshooting A4 Sweeper PCB.

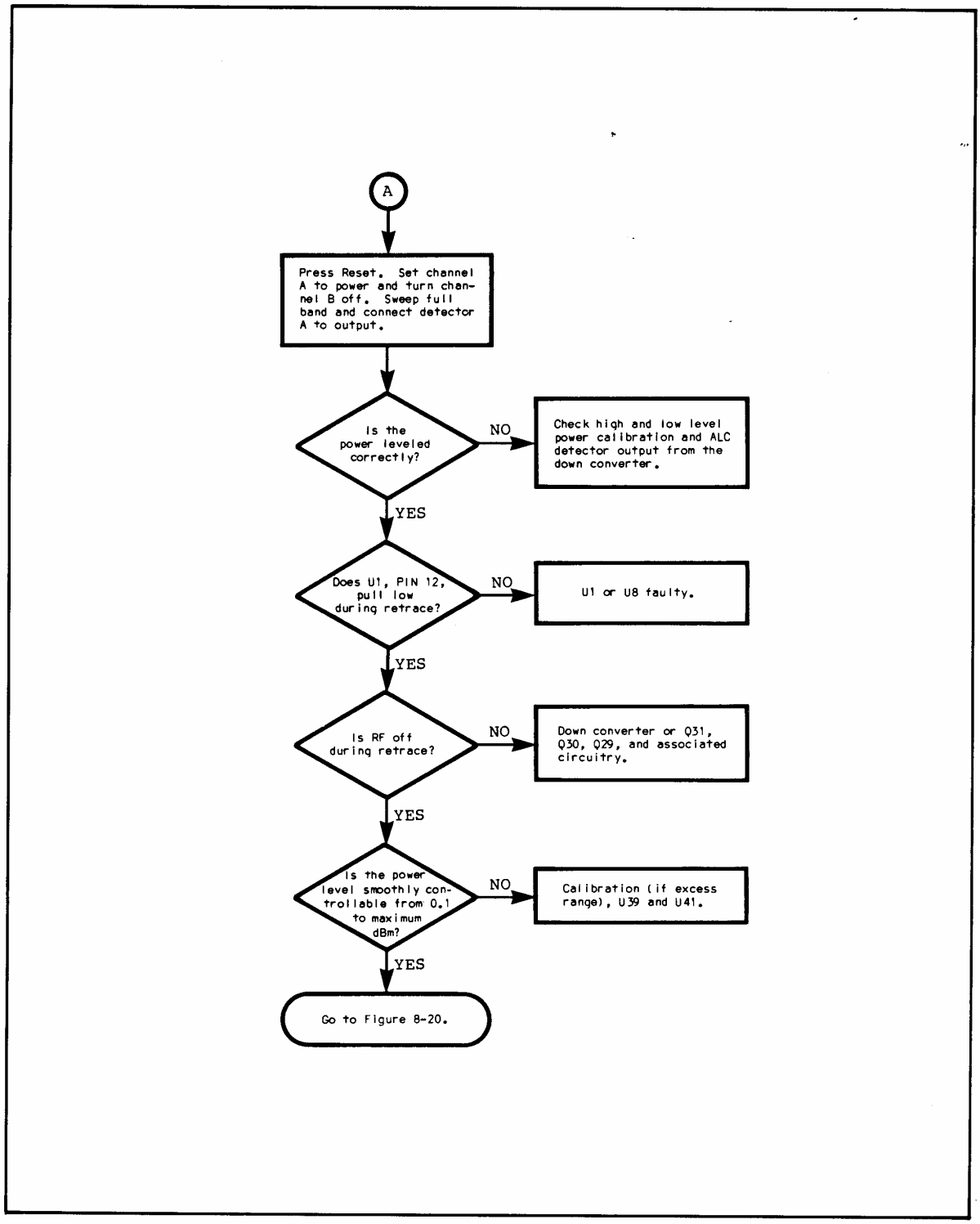


Figure 8-15. Troubleshooting A4 Sweeper PCB (continued).

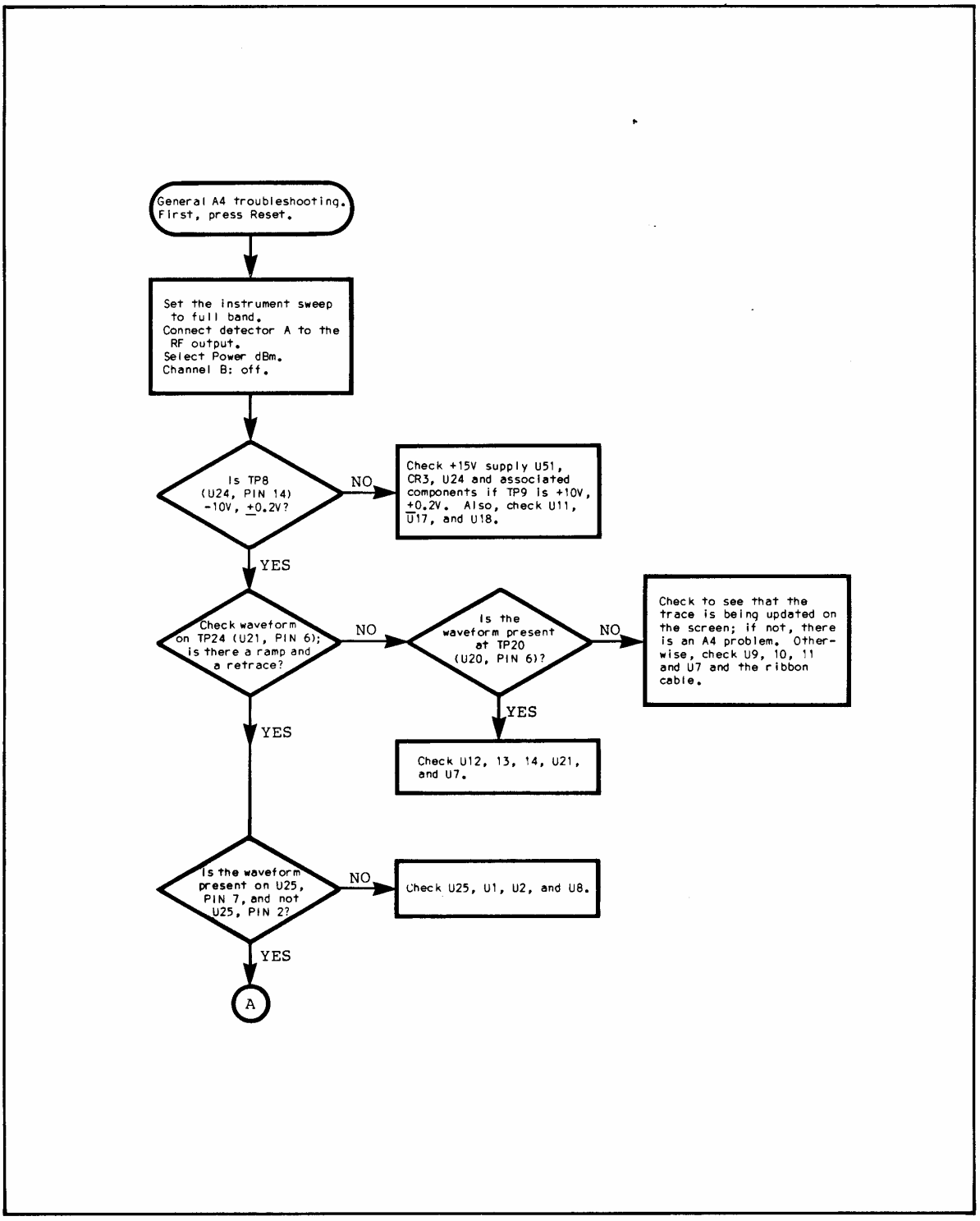


Figure 8-16. Further A4 Troubleshooting.

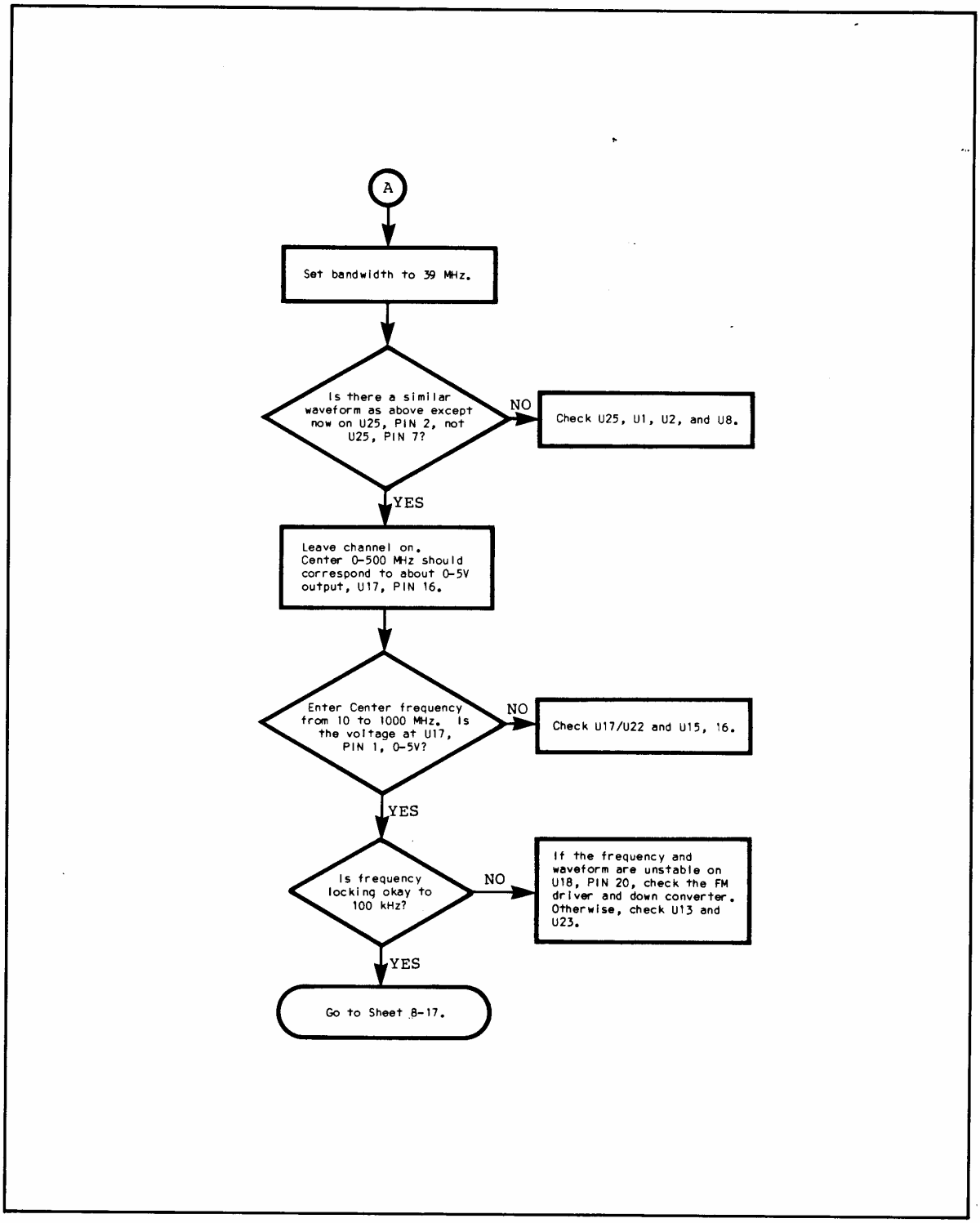


Figure 8-16. Further A4 Troubleshooting (continued).

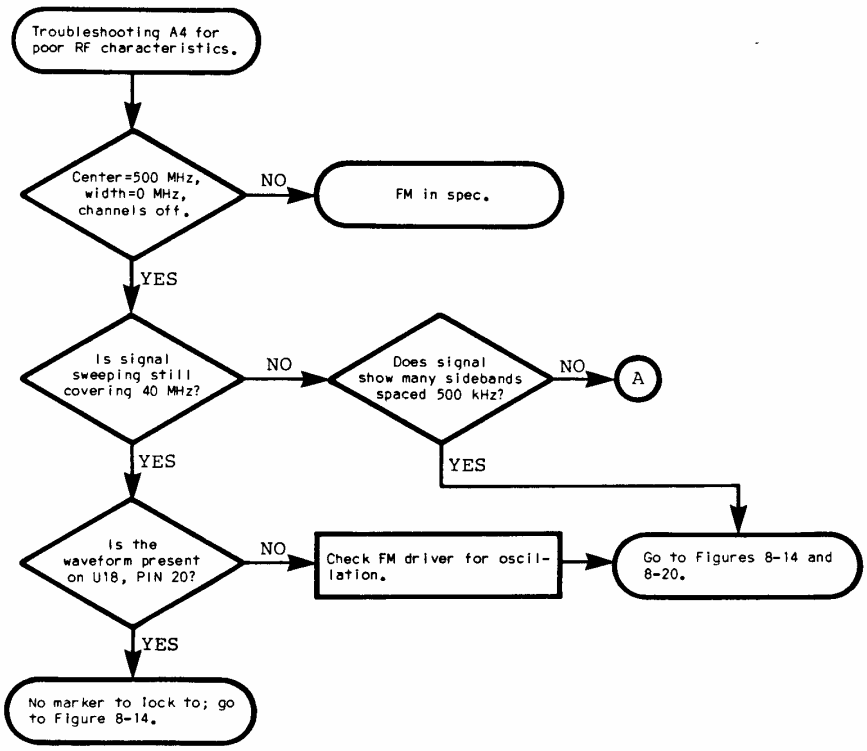


Figure 8-17. Troubleshooting A4 with Poor RF Characteristics.

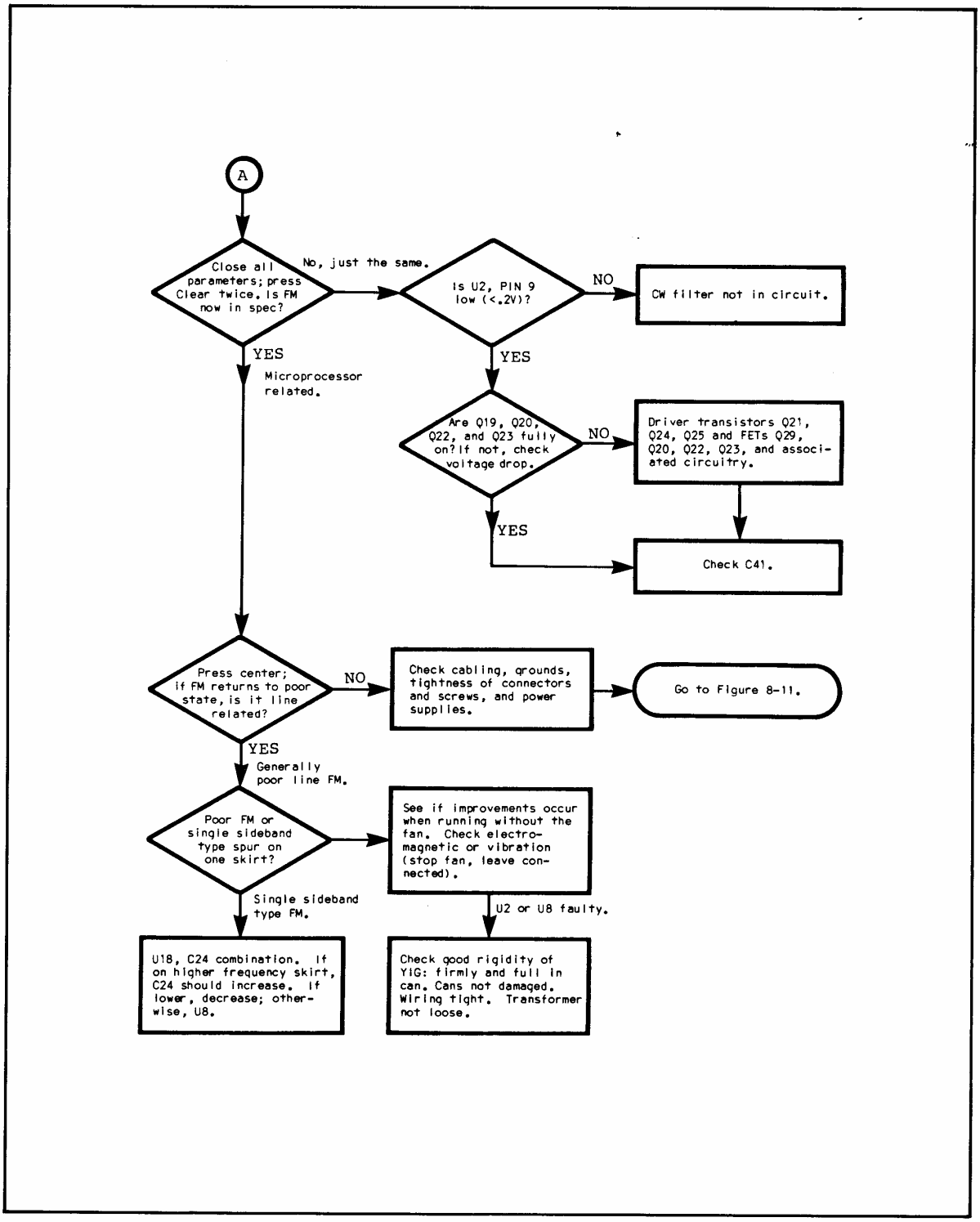


Figure 8-17. Troubleshooting A4 with Poor RF Characteristics (continued).

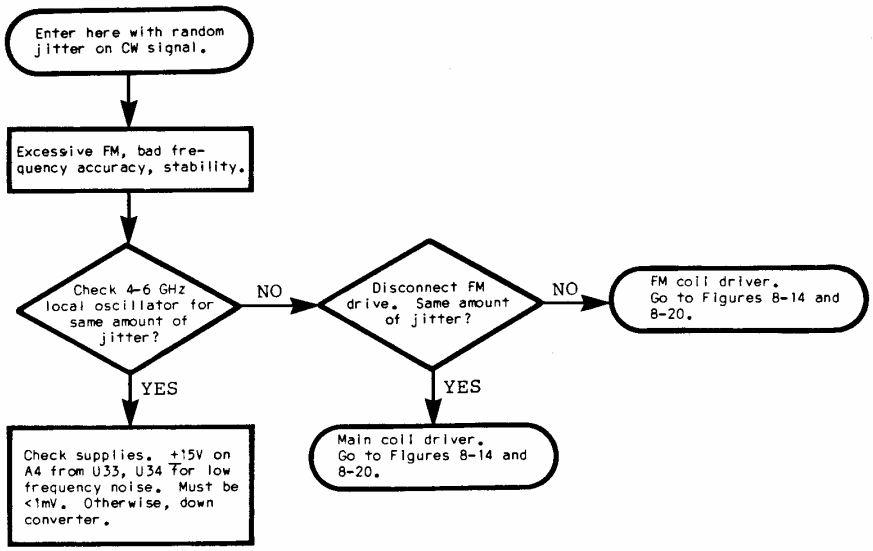


Figure 8-17. Troubleshooting A4 with Poor RF Characteristics (continued).

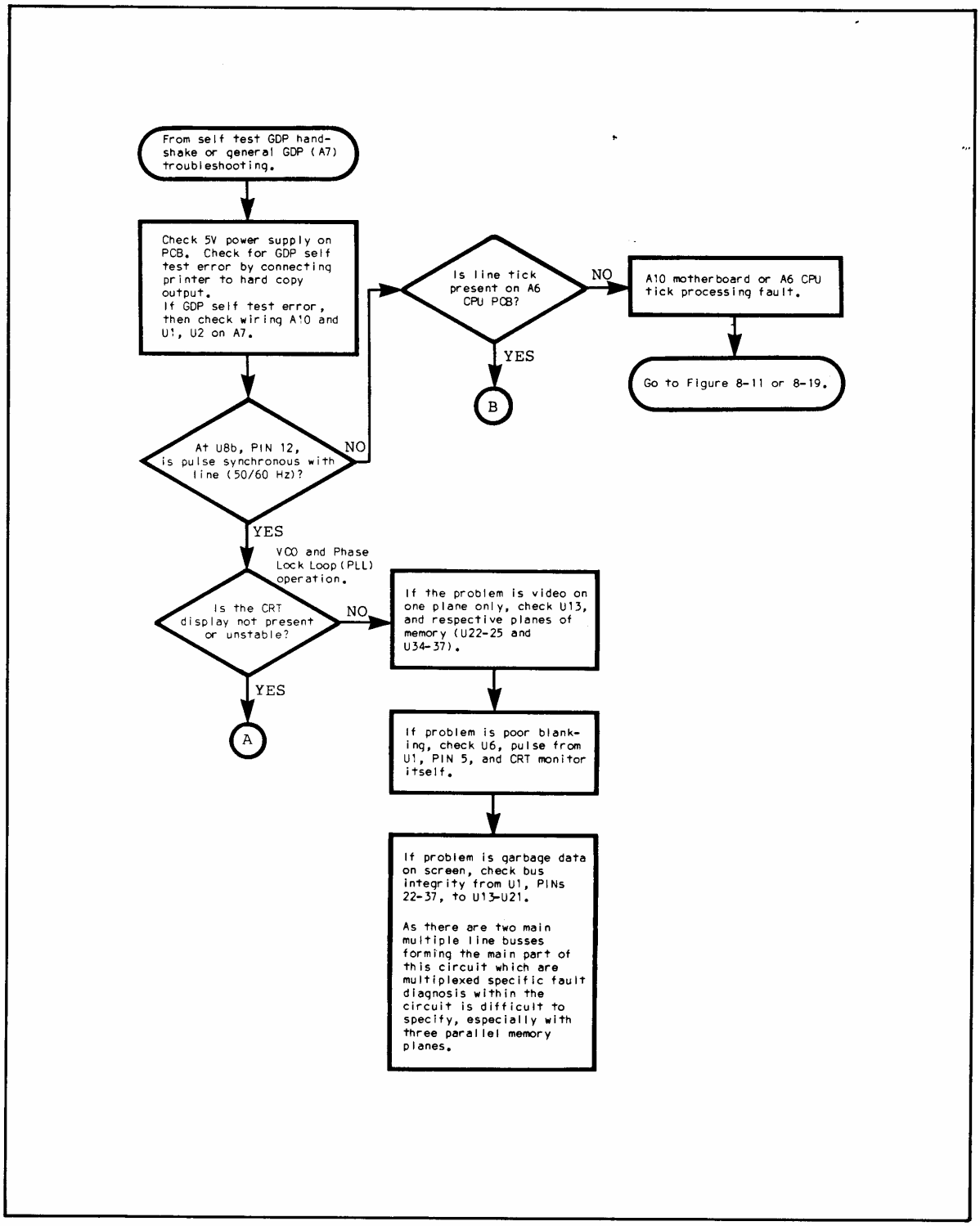


Figure 8-18. Troubleshooting A7 Graphic Display Processor (GDP).

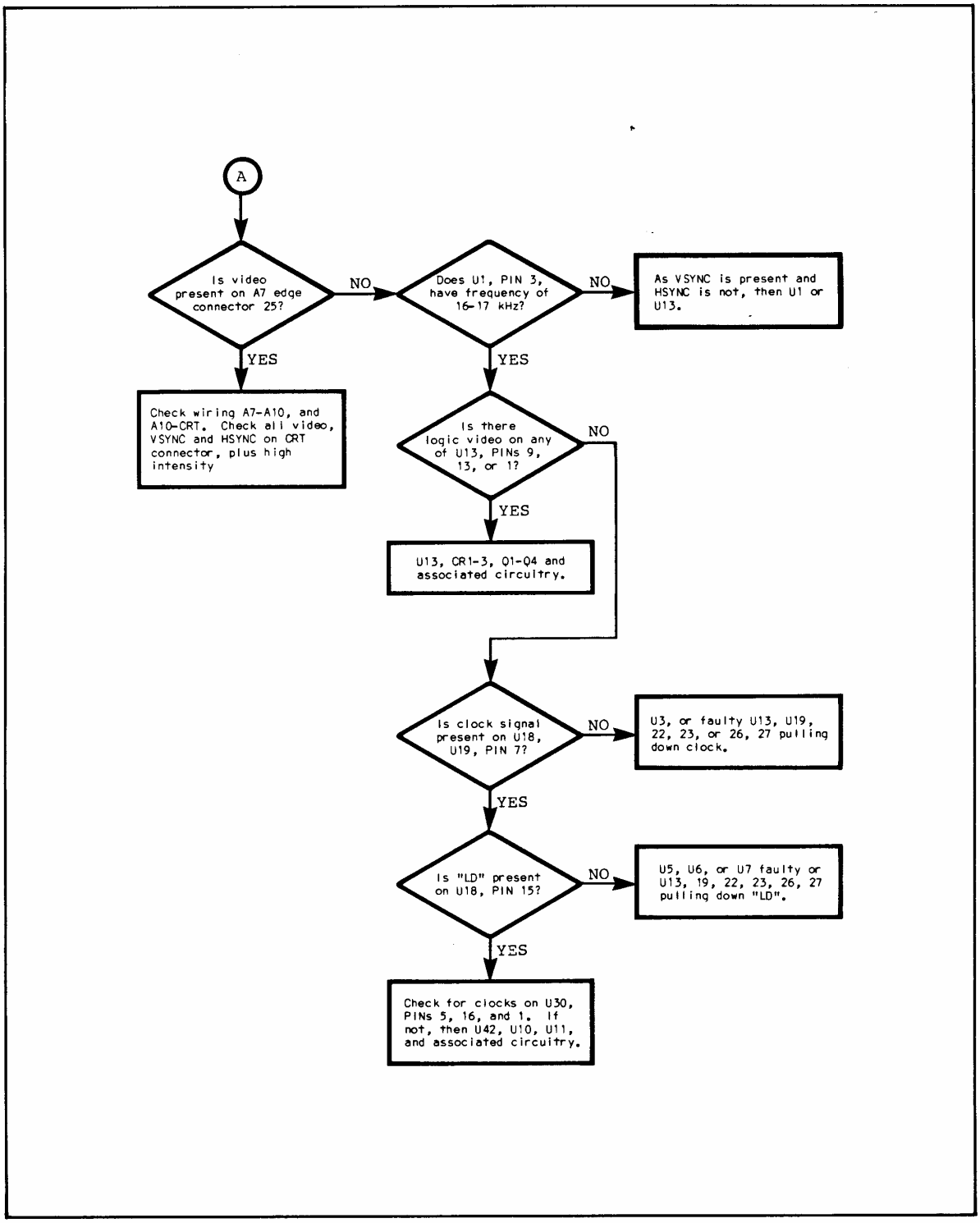


Figure 8-18. Troubleshooting A7 GDP (continued).

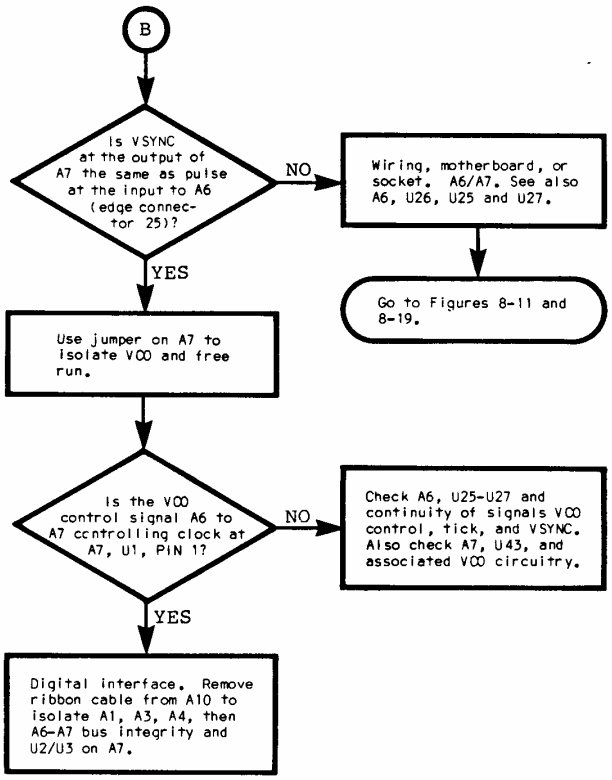


Figure 8-18. Troubleshooting A7 GDP (continued).

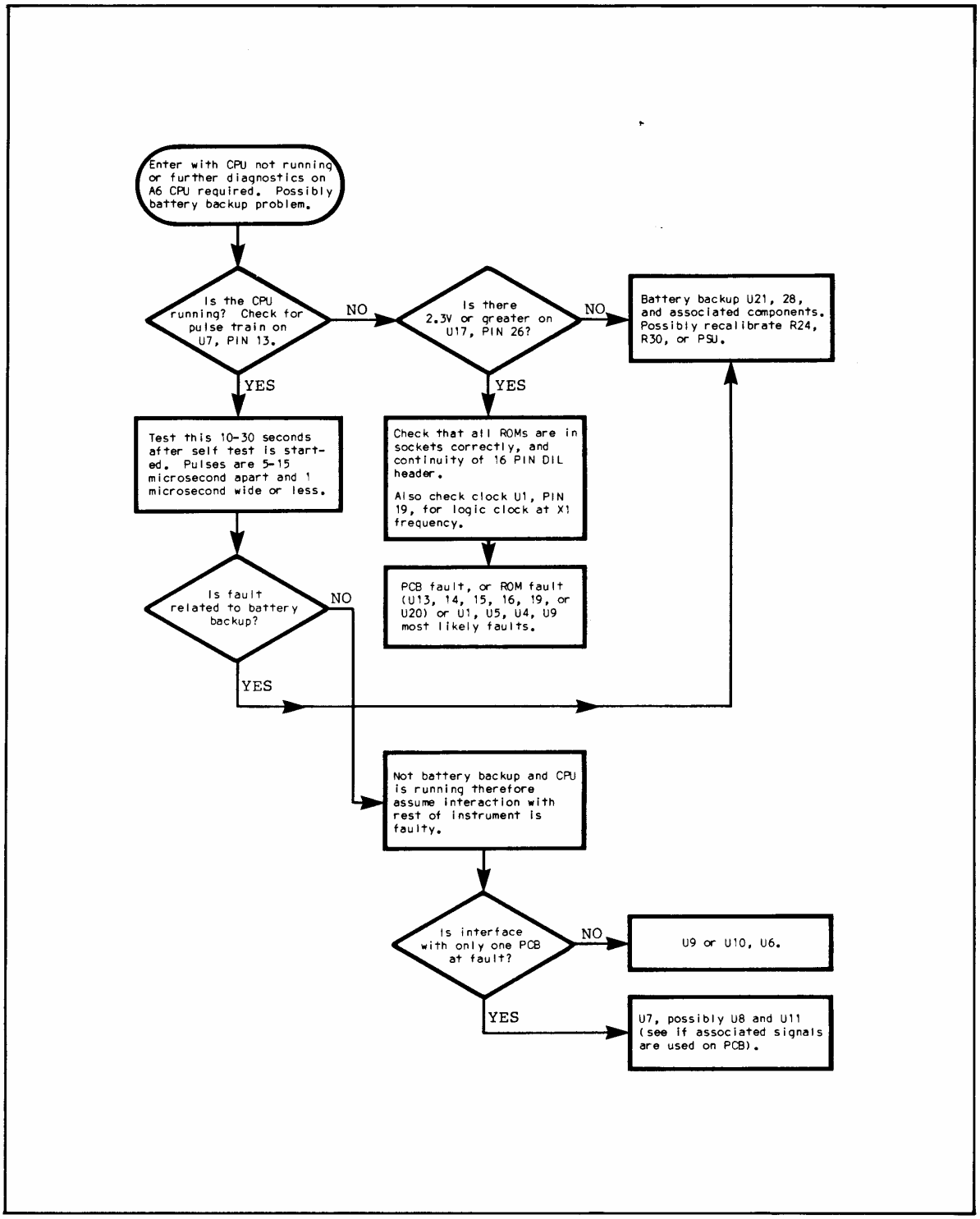


Figure 8-19. Troubleshooting A6 CPU.

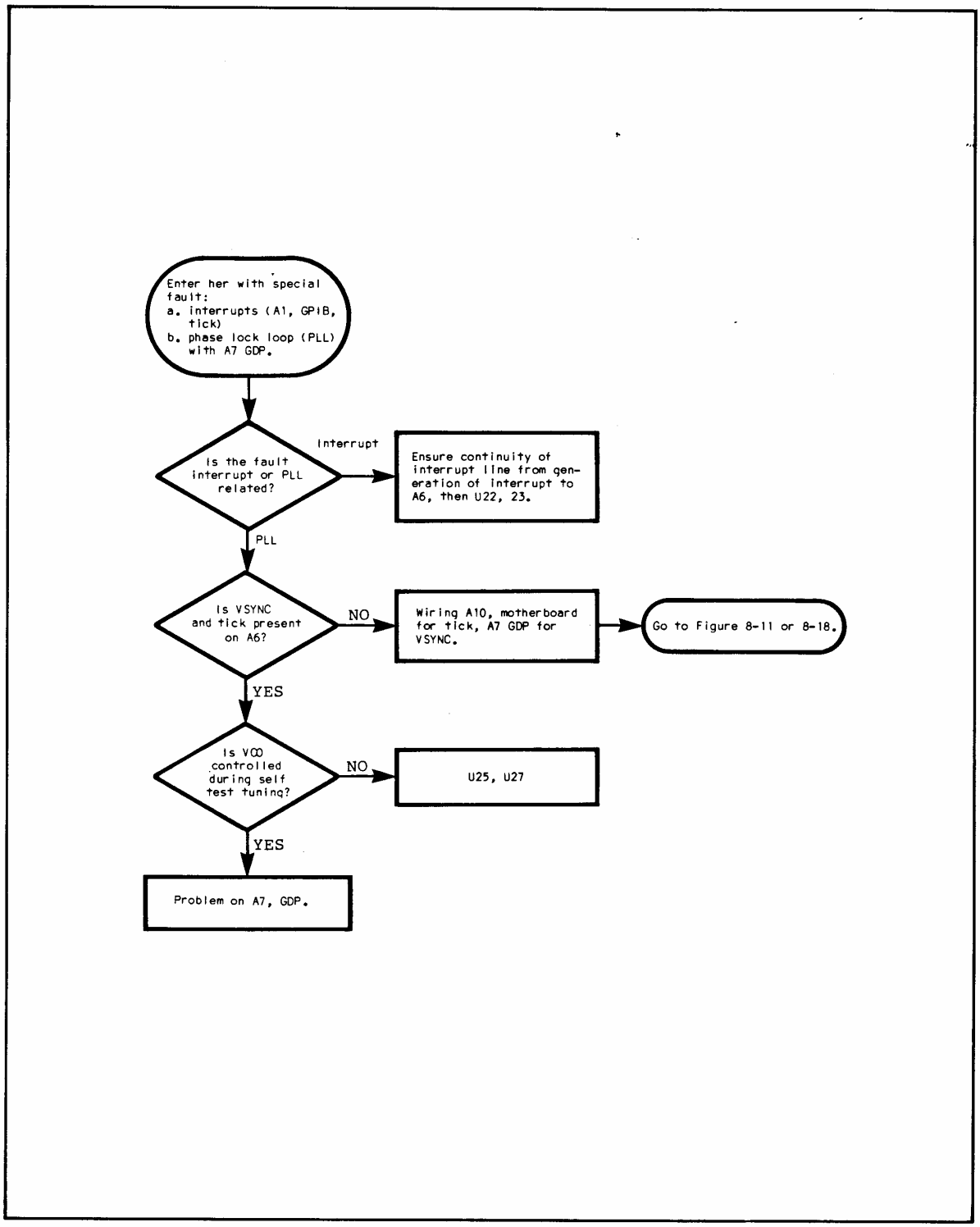


Figure 8-19. Troubleshooting A6 CPU (continued).

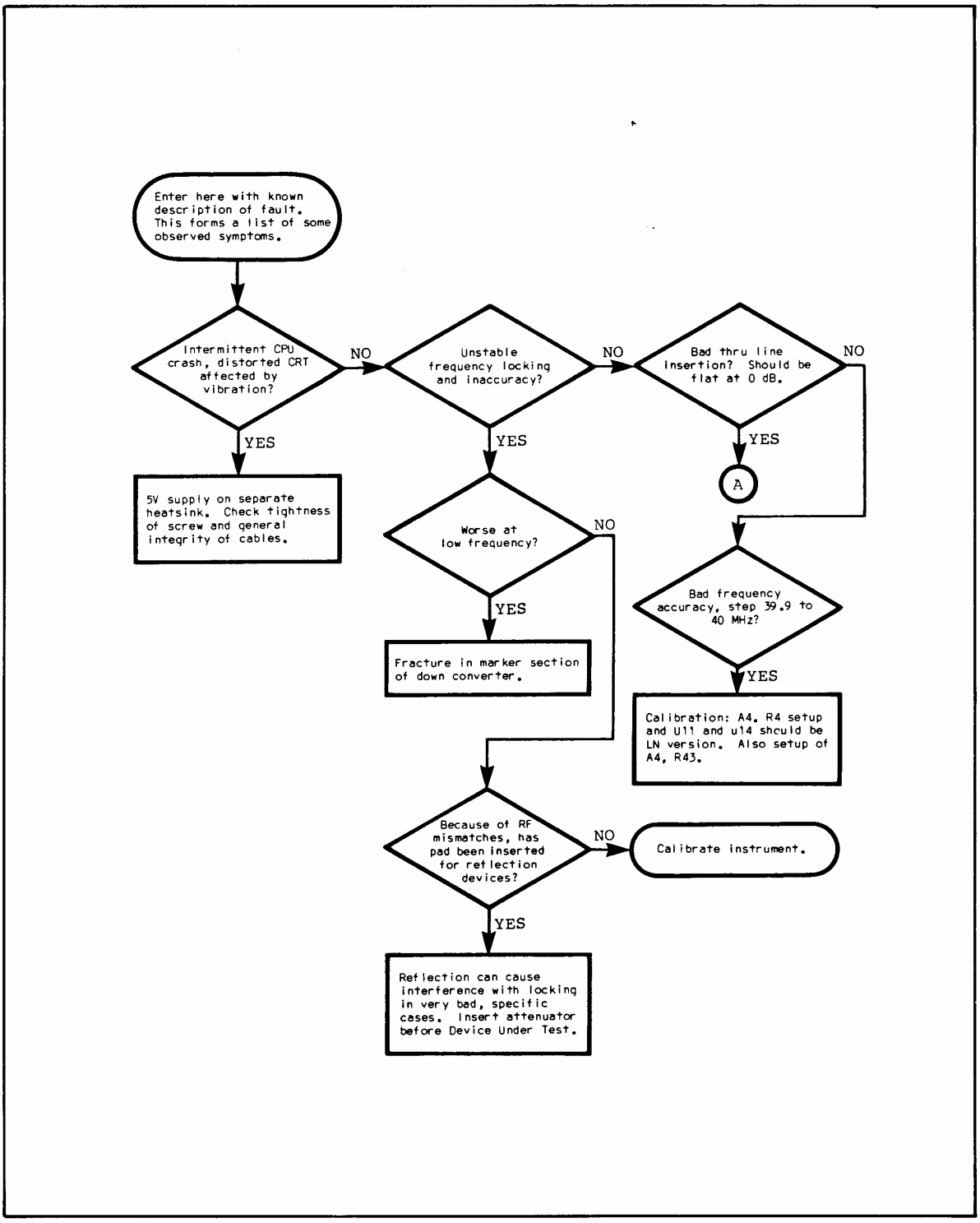


Figure 8-20. Symptom Sorter.

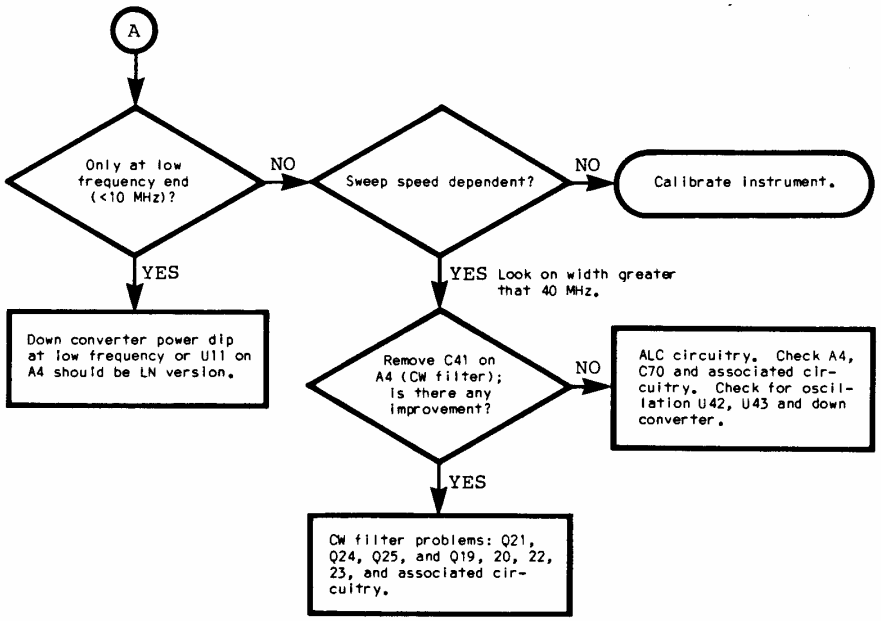


Figure 8-20. Symptom Sorter (continued).

8-7 6400 CIRCUIT DESCRIPTIONS

8-7.1 Circuit Overview

The 6407/6409 RF Analyzer consists of a digital scalar network analyzer and a frequency locked sweeper. The operation of the instrument is controlled by a 16-bit microprocessor (the CPU) located on the A6 PCB. The RF Analyzer functional block diagram is shown in Figure 8-21.

a. The A6 CPU. The CPU directly accesses the graphics display processor (GDP), the Centronics printer interface, and the GPIB. The CPU also connects, via the ribbon bus through the A10 Motherboard, to the A4 Sweeper PCB, the A3 Signal Channel PCB, and the A1 and A11 control panel PCBs. The CPU communicates using an 8-line data bus.

   The CPU holds the main processor, the operating system in EPROM and PERSONALITY EPROM, and the RAM. The main bus is routed to the edge connector of the A6 PCB for distribution to other PCBs.

b. A4 Sweeper PCB. Located underneath the RF deck, the A4 board controls frequency for both the main coil and the FM coil, and controls the source power level. The board contains a digital interface to the CPU, DACs with latches to provide the signals to the YIG drivers, and ALC circuitry.

c. RF Deck. The RF deck holds the YIG oscillator, the source of all RF signals. The RF from the oscillator output connects directly to a low pass filter (contained within the oscillator package), which removes harmonics.

   The RF then travels to the down converter/marker pack. As the RF enters the down converter, it passes through a PIN diode, which is used for attenuation. Inside the down converter, the RF signal is mixed with a local oscillator to produce the down converted signal for the instrument's RF output.

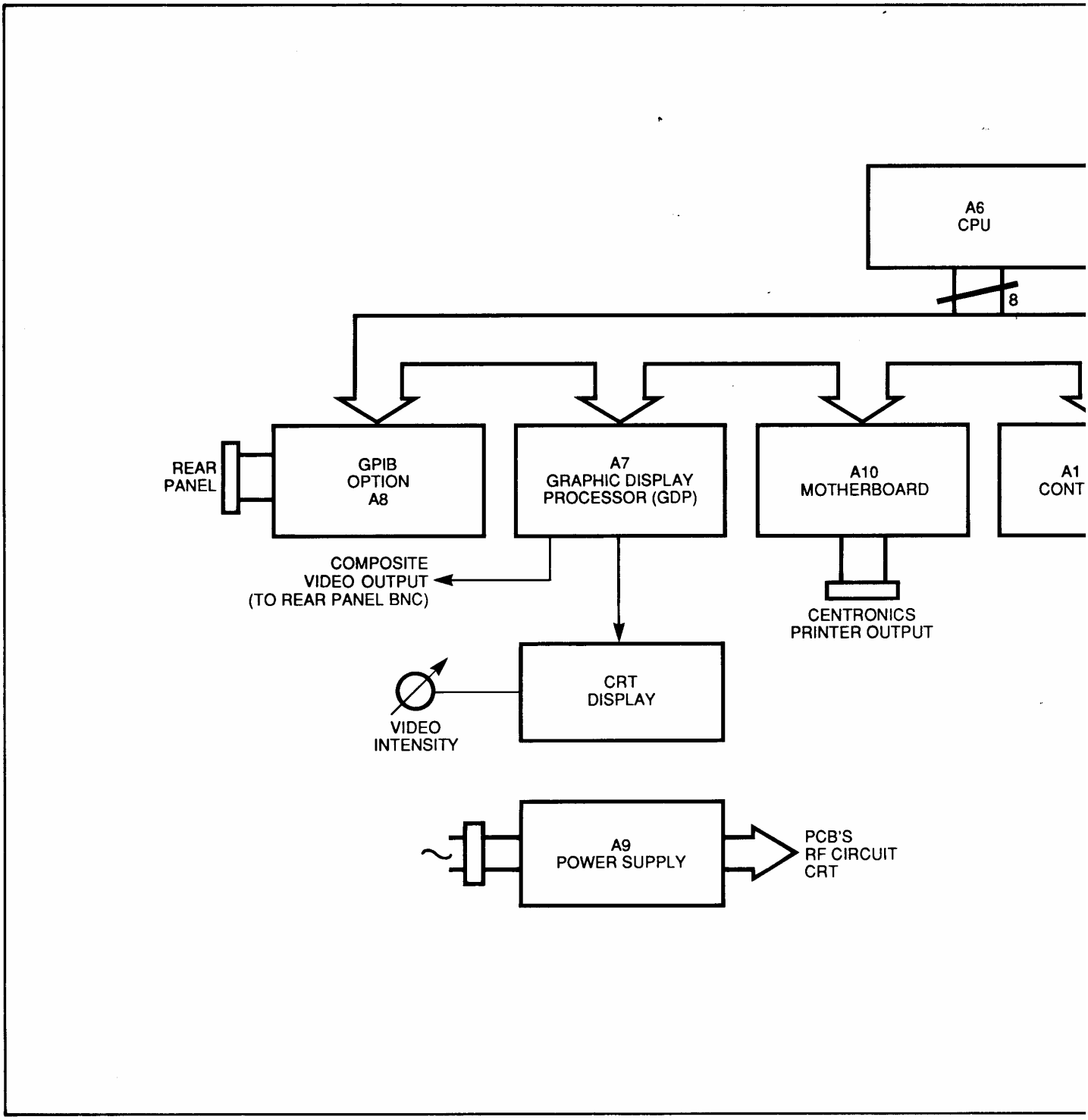
   A signal sample is also mixed with another oscillator, forming the basis of the marker locking. This signal is routed out of the down converter as the marker signal. The down converter also provides a signal for the automatic level control (ALC).

   The optional attenuator located on the RF deck, provides attenuation in 10 dB steps up to a maximum of 70 dB. The attenuator is controlled by relay drivers on the A4 PCB.

d. A3 Signal Channel. The A3 signal channel's primary function is to amplify the incoming test signal to a suitable level for analog-to-digital conversion (ADC) and to present either linear or logarithmic data to the A6 CPU. The detected voltage coming into the A3 board is via the channel A and channel B inputs.

   Temperature and square law deviation characteristics of the detector/autotester are also processed on A3. The thermistor, log conformity, and the actual detected signal are read by switching the input of the ADC on A3. The autozero function is performed by the signal channel under the control of the A6 CPU during sweeper retrace.

e. A1 and A11 Control Panel PCBs. The control panel PCB (A1) holds the matrix of control panel keys, with an extension PCB (A11) for the keys under the CRT. When a key is pressed, an individual code and an interrupt for the A6 microprocessor is generated. All control panel LEDs are controlled by the CPU except for the unleveled LED, which is directly controlled by the A4 sweeper board.


A6
CPU
8
REAR
PANEL
GPIB
OPTION
A8
A7
GRAPHIC DISPLAY
PROCESSOR (GDP)
A10
MOTHERBOARD
A1
CONT
COMPOSITE
VIDEO OUTPUT
(TO REAR PANEL BNC)
CENTRONICS
PRINTER OUTPUT
CRT
DISPLAY
VIDEO
INTENSITY
A9
POWER SUPPLY
PCB'S
RF CIRCUIT
CRT

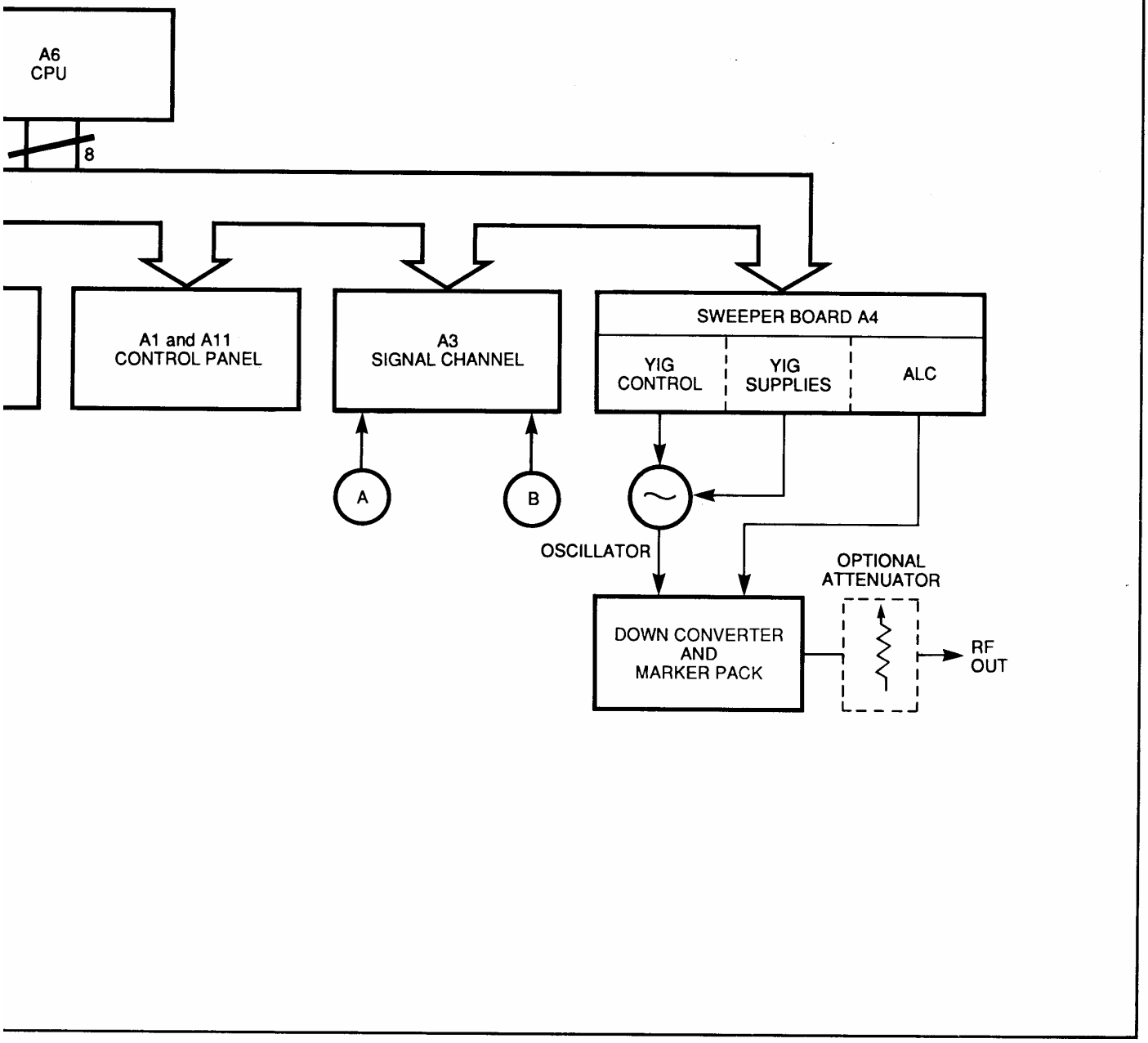


Figure 8-21. 6400 Overall Block Diagram

The action of the analog, or spinwheel, knob is encoded to provide interrupts indicating direction of knob rotation. When the knob is rotated the CPU decodes the frequency of interrupts and makes the corresponding parameter changes.

f. A7 Graphics Display Processor. The primary functions of the GDP are to:
   1. accept instructions from the CPU for updating the trace information.
   2. display characters that make up the prompts and menus.
   3. display other graphic information, such as markers.
   4. continually read out the whole contents of all three memory planes at the frame rate of the CRT display.

   The A7 GDP takes commands from the CPU to control access to the three graphic memory planes. The memory planes display:
   1. Alphanumerics, graticule, limits, and markers.
   2. Channel A trace and identifying letter.
   3. Channel B trace and identifying letter.

g. CRT and Driver Board. Video and sync information as well as the 12V supply enter the CRT driver board via the edge connector. The high voltage supply (12 kV) is generated on the board.

   The display frame rate is automatically locked to the line frequency (50 or 60 Hz). The locking is performed by a phase-lock loop. Circuitry on A6 generates a voltage for the voltage controlled oscillator (VCO) on the A7 GDP. This oscillator provides the main clock for the CRT driver board.

h. A9 Power Supply. The power supply consists of a toroidal transformer, bridge rectifiers, and regulators. The supply is protected from overload by current-limiting polyswitches. If the current in the circuit increases, the impedance of these polyswitches increases, hence limiting the current.

   The power supply provides the 5V logic supply, general ±15V supplies, 12V CRT supply, and the supplies for the YIG and down converter.

i. A8 GPIB. This option consists of a dedicated GPIB processor and GPIB driver chips. All interface to the CPU is via interrupts generated by the GPIB chip.

8-7.2 A1 Control Panel PCB

The A1 control panel PCB, which is attached to the back of the control panel, provides the mechanical support for the control panel pushbuttons. A1 also performs priority encoding and interrupt generation for the pushbuttons. The ribbon bus carries data for the control panel indicators (LEDs) and from the spinwheel analogue control, as well as power for the PCB.

The A1 control panel block diagram is shown in Figure 8-26. The A1 parts locator diagram and A1/A11 schematic are shown in Figures 8-27 and 8-28. Unless otherwise directed, refer to the block diagram, Figure 8-26, for the following discussions.

a. Pushbutton Matrix System. The pushbutton matrix system identifies which button on the control panel has been pressed. Control panel switches and LEDs are shown in their respective positions in Figure 8-22. Table 8-5 lists each switch and its associated function.

The control panel pushbuttons are wired into an X-Y matrix. Since, both the X and the Y lines are numbered in the range of zero to seven, there are 64 possible matrix locations. Only 41, however, are used by the control panel. Four locations are occupied by the A11 subsidiary control panel: two X lines and two Y lines go to connector P2, along with a ground line.

Both the X and Y lines are pulled to a logic HIGH (+5V) by 10 kΩ resistors, R40 thru R55 (Figure 8-28, Schematic). When a control panel button is pressed, that particular button's X and Y line is tied to ground. This defines each button's position in the matrix.

The eight Y-matrix lines go to U2, an eight-to-three line priority encoder, as shown in Figure 8-23. When any of the eight input lines go to logic 0 (ground), U2 produces a three bit binary encoded number in the zero to seven range. This number corresponds to the selected

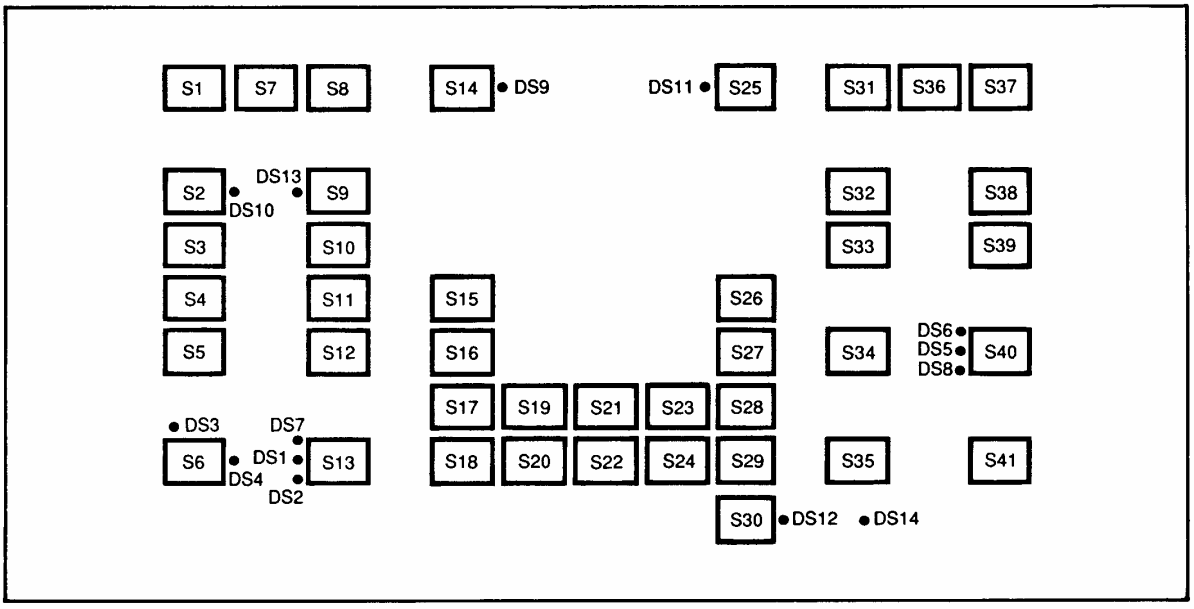


Figure 8-22. Control Panel Switches and LEDs

Table 8-5. Control Panel Switches/Functions

Switch Number	Function	Switch Number	Function
S1	Save Recall	S22	Data Entry "8"
S2	Channel A Display ON/OFF	S23	Data Entry "4"
S3	Channel A Offset Resolution	S24	Data Entry "9"
S4	Channel A Autoscale	S25	Return to Local
S5	Channel A Menu	S26	Data Entry "Enter"
S6	Calibration	S27	Data Entry "Clear"
S7	Self Test	S28	Data Entry "5"
S8	Reset	S29	Data Entry "0"
S9	Channel B Display ON/OFF	S30	RF ON/OFF
S10	Channel B Offset Resolution	S31	Hard Copy Menu
S11	Channel B Autoscale	S32	Source Frequency START
S12	Channel B Menu	S33	Source Frequency CENTER
S13	Smoothing	S34	Markers
S14	Hold	S35	Source Frequency Menu
S15	Data Entry "-"	S36	Hard Copy Start Print
S16	Data Entry "."	S37	Hard Copy Stop Print
S17	Data Entry "1"	S38	Source Frequency STOP
S18	Data Entry "6"	S39	Source Frequency Width
S19	Data Entry "2"	S40	Frequency Data Points
S20	Data Entry "7"	S41	Power Level
S21	Data Entry "3"		

input. If two inputs are received simultaneously, U2 selects the code from the highest priority line to be represented on the output. When a valid code is found, U2 produces a logic 0 signal on its EO output (pin 15).

The eight X-matrix lines go to U1, which is also a priority encoder. U1 handles signals similarly to U2.

When a control panel pushbutton is pressed, the two EO signals from U1 and U2 are ANDed together by CR4 and CR5. The resulting signal is connected to bit 4 of data port 20H (U4, a tri-state buffer). The CPU then:

1. Reads the signal and the matrix data.
2. Allows the time for which the key was pressed to be measured.
3. Allows suitable software debouncing action to take place.

The keycode information therefore is read through Port 20H (U4). All port addresses are decoded by U7. From U4, bits zero to two are connected to U2 and receive the Y line information. Bits three to five are connected to U1 and receive the X line information. This provides a six-bit code uniquely identifying each switch.

The ANDed EO signals from U1 and U2 are also used to trigger latch U3A, which activates the $\overline{INT_3}$ line on the ribbon bus and interrupts the central processor. This interrupt signal is cleared by any read to Port 20H (U4). A momentary low on U3A, pin 1, will clear the latch. Since U3 is edge triggered, no further key interrupt can occur until the button is released and EO goes to logic HIGH.

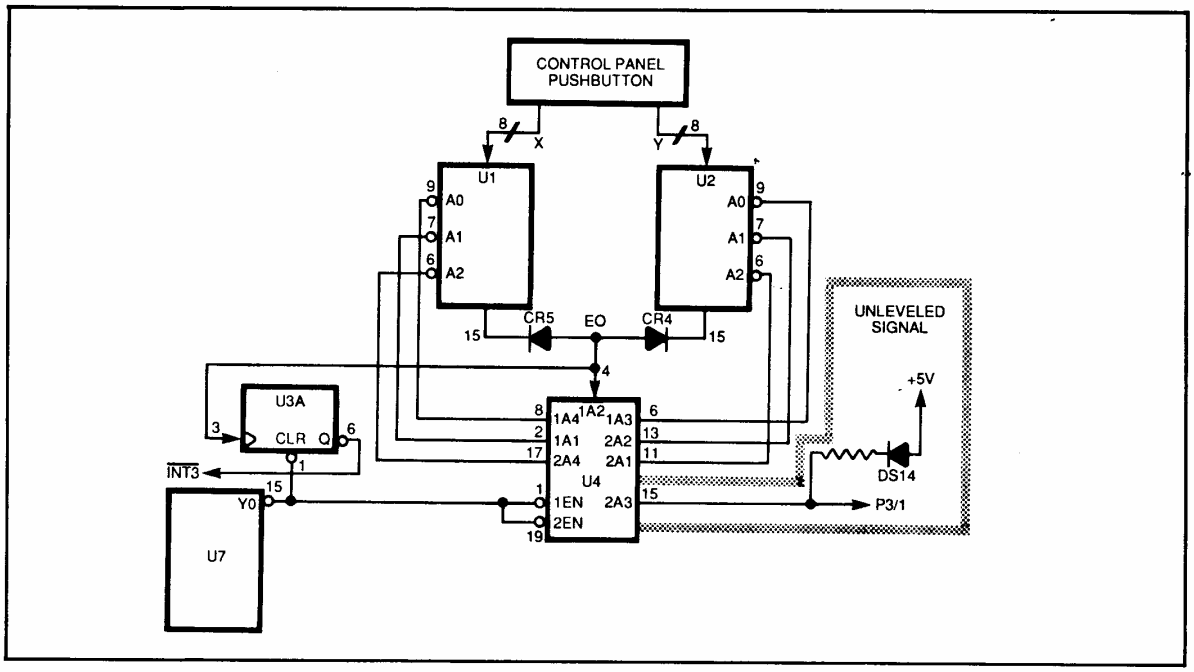


Figure 8-23. Pushbutton Matrix System

Data bit seven of U4 is not needed by the pushbutton matrix system. It is used to let the processor know whether the instrument's RF output power is leveled or unleveled. The unleveled signal comes from the A4 PCB and goes to P3-1 of A1. Pin 2 of P3 is unallocated. When the instrument is in an unleveled condition, this signal goes to a logic LOW, causing the indicator DS17 to illuminate and the signal to appear on bit seven of U4.

The A11 subsidiary control panel interfaces with the pushbutton matrix system via connector P2. Table 8-6 shows the pin numbers and associated signal lines.

b. Indicators. LED indicators on the control panel provide information about selected parameters.

Octal data latch U6 (Figure 8-24) drives eight indicators, DS1 thru DS8. Data latch U6 has a port address of 23H and is decoded by U7. Indicators DS9 thru DS13 are driven from octal latch, U5, which has a port address of 21H, and is also decoded by U7.

Table 8-6. P2 Connector to A11 PCB

Pin No.	Signal
1	+5V (not used)
2	X1 Scan Matrix row
3	X5 Scan Matrix row
4	Y5 Scan Matrix column
5	Y6 Scan Matrix column
6	0 V (Digital Ground)

The remaining indicator, DS14 (Figure 8-23), receives its drive directly from the A4 sweeper board thru connector P3.

Table 8-7 shows the LED port addresses and the associated indicator definition.

Table 8-7. LED Ports

Bit	Port	LED	Indication
0	23H	DS8	401 Data Points
1	23H	DS7	Smoothing Off
2	23H	DS5	201 Data Points
3	23H	DS6	101 Data Points
4	23H	DS4	Begin Calibration
5	23H	DS3	Uncalibrated
6	23H	DS2	Smoothing Max
7	23H	DS1	Smoothing Min
0	21H		Unallocated
1	21H		Unallocated
2	21H	DS10	Channel A On
3	21H	DS11	Remote (GPIB)
4	21H	DS9	Hold
5	21H	DS13	Channel B On
6	21H	DS12	RF Off
7	21H		Clear Spinwheel Interrupt

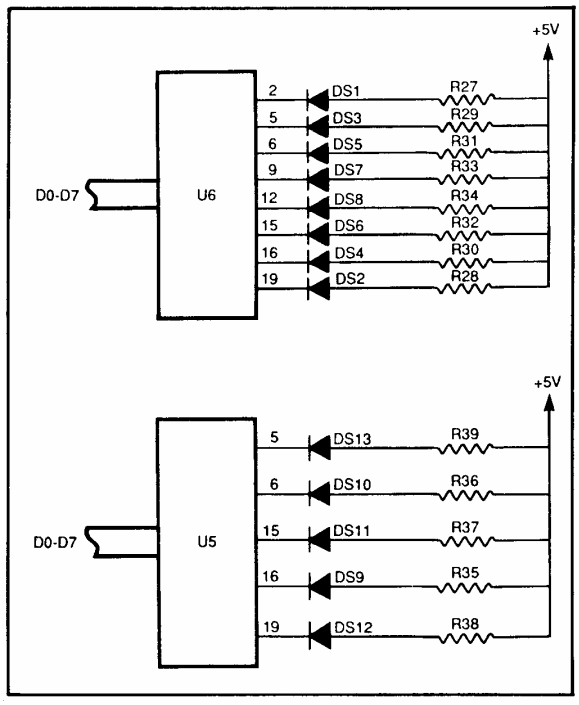


Figure 8-24. LED Indicators

c. Spinwheel. The spinwheel knob in the data entry section of the control panel provides analogue control over instrument parameters.

The knob is attached to the shaft of a small, DC electric motor which is used as a generator. This generator produces a positive voltage if the knob is rotated in one direction and negative voltage if it is rotated in the opposite direction. The magnitude of the voltage produced is proportional to how quickly the knob is rotated.

P4 provides the electrical connection between the spinwheel assembly and the control panel. A simplified schematic of this circuitry is shown in Figure 8-25. The signal voltage at this point contains information about speed and direction of rotation of the spinwheel. This information is then converted to a series of pulses that interrupt the CPU via U9 and U10, together with Q1 thru Q4.

Operational amplifier U9 and its associated circuitry form an integrator that can be reset by turning on Q1. When the knob is rotated, the signal at the input of U9 causes the output of the integrator to become more- or less-positive. This signal is dependent upon the direction of rotation to the magnitude of the signal. The magnitude of the signal is proportional to the speed of rotation of the spinwheel.

The output of U9 goes to a window comparator, U10, that has a logic HIGH trip of +8V and a logic LOW trip of +7V. When the spinwheel is not being turned, the output voltage of U9 is at +7.5V, which is at the midpoint of the window comparator.

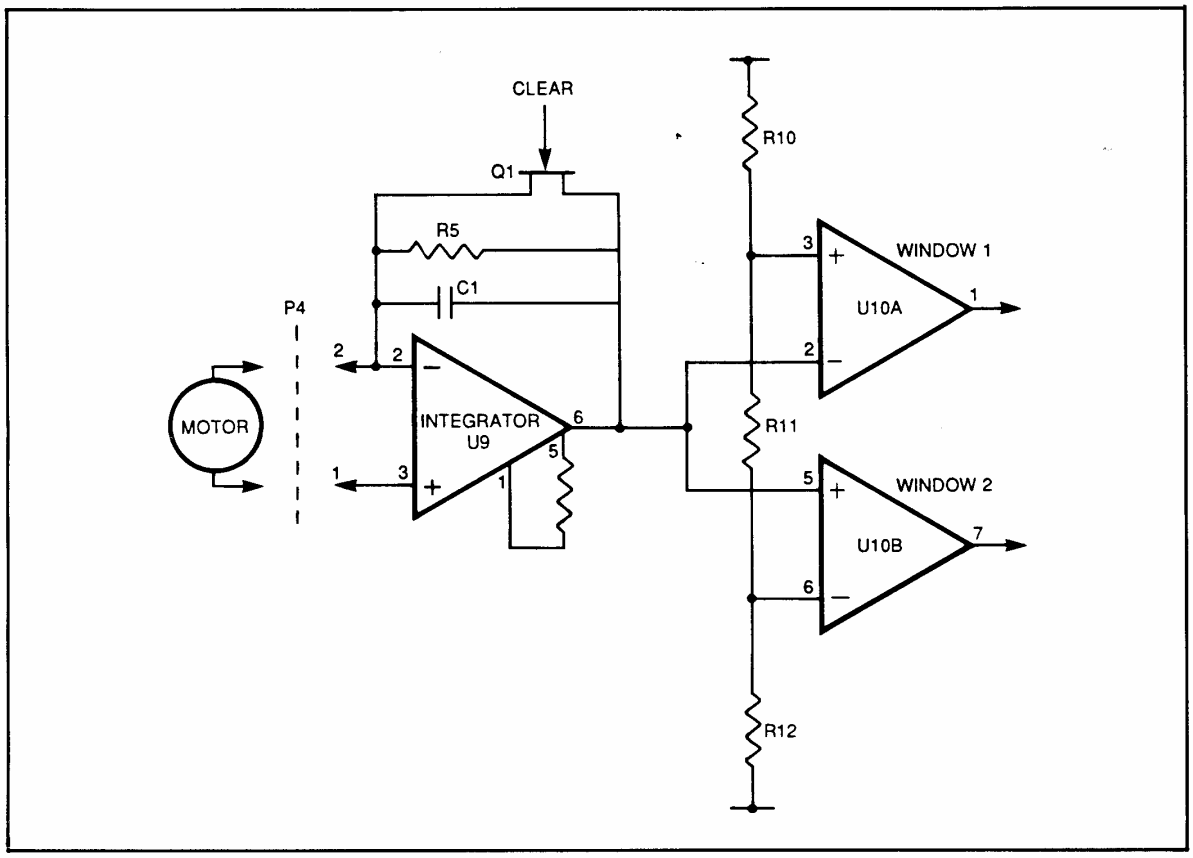
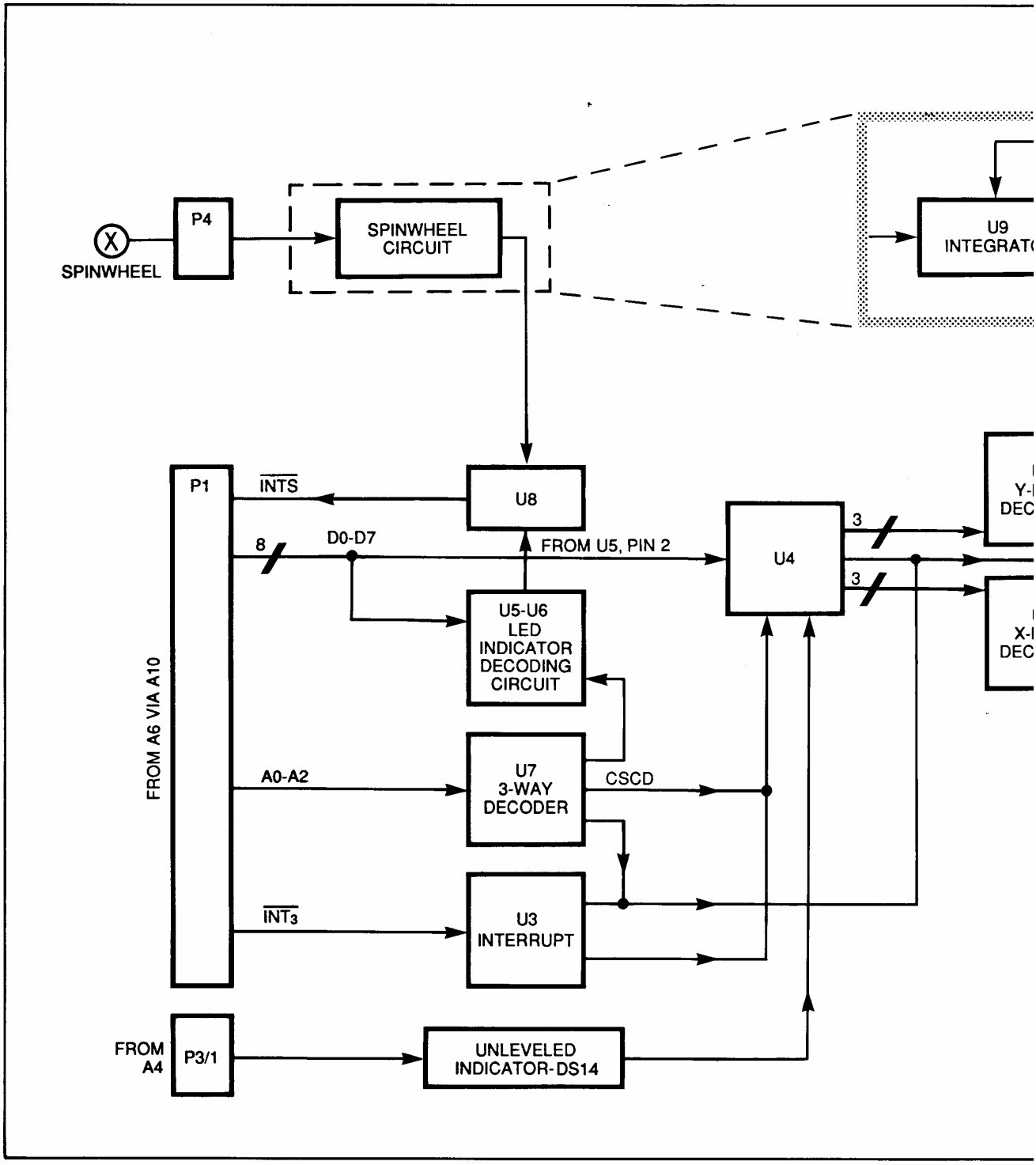


Figure 8-25. Spinwheel Operation

Rotation of the spinwheel causes the U9 output to rise or fall until it lies outside the comparator window. This causes the comparator output to go to a logic LOW. Q2 then generates a pulse sufficient to turn on Q1, which discharges C1, and thus resets the integrator. If the spinwheel is still being turned, the whole process repeats.

The relevent output of the comparator consists of a train of negative going pulses with a repetition rate proportional to the speed of rotation of the spinwheel. If the knob is rotated in a clockwise direction, pulses are output at pin 1 of U10. To interface with the CPU, these pulses are level-translated by Q4 and used to trigger interrupt latch U8, forcing a knob increment interrupt. This function is reset by the CPU using a line from one of the LED drivers (Bit 7, port 20H).

When the knob is rotated in a counter clockwise direction, a similar process occurs with the other comparator. The pulses then appear on pin 7 of U10 and are level-translated by Q3. A knob increment interrupt is generated by the other latch in U8 and is reset as described above.


SPINWHEEL
P4
SPINWHEEL CIRCUIT
U9
INTEGRAT
P1
INTS
U8
8
D0-D7
FROM U5, PIN 2
U4
3
3
Y-
DEC
X-
DEC
U5-U6
LED
INDICATOR
DECODING
CIRCUIT
FROM A6 VIA A10
A0-A2
U7
3-WAY
DECODER
CSCD
INT3
U3
INTERRUPT
FROM
A4
P3/1
UNLEVELED
INDICATOR-DS14

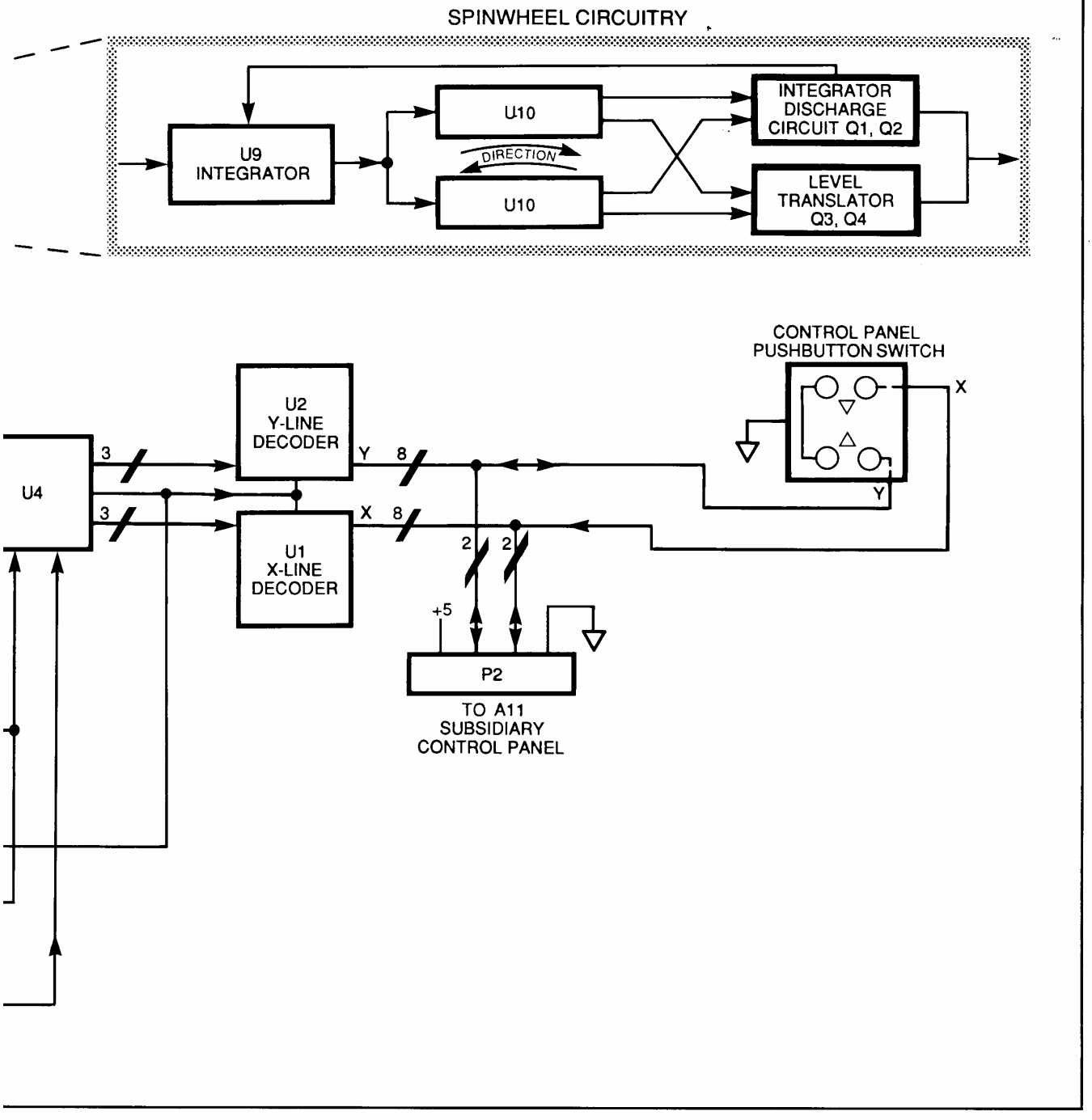


Figure 8-26. A1 Control Panel Block Diagram

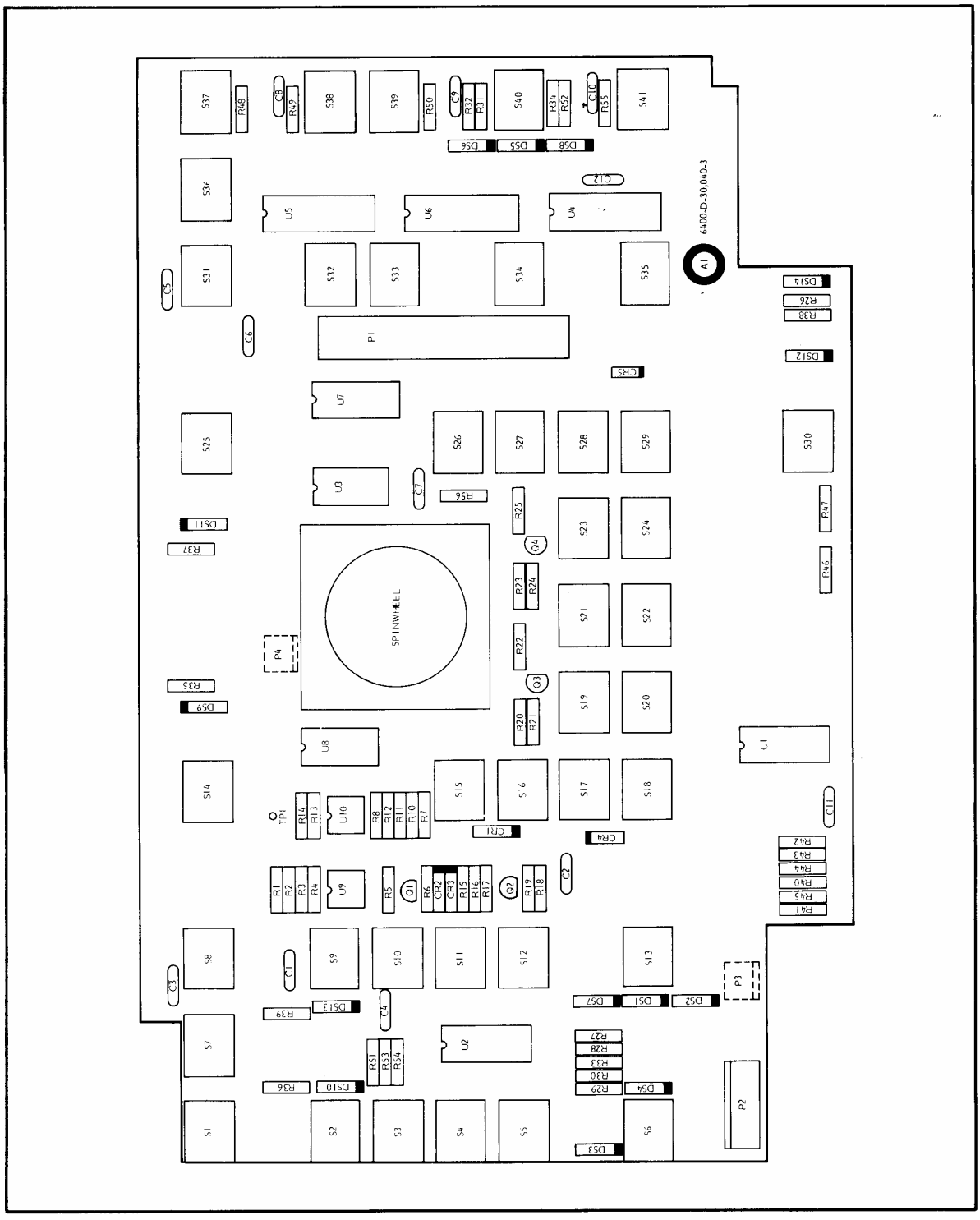
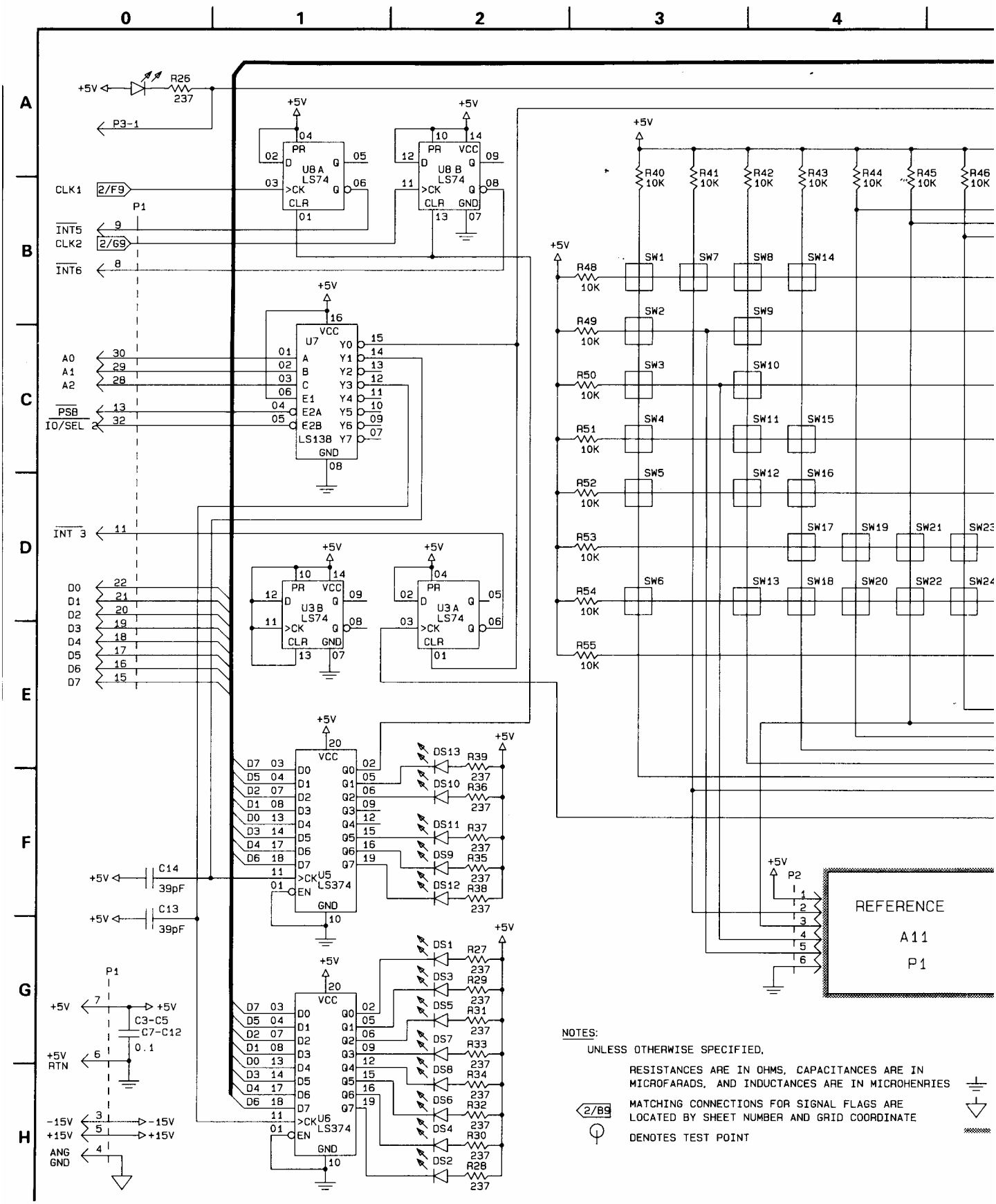


Figure 8-27. A1 PCB Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
+5V
R26
237
P3-1
CLK1
2/F9
P1
INT5
CLK2
2/G9
INT6
U8 A
LS74
U8 B
LS74
PR
CLR
>CK
D
Q
VCC
GND
A0
A1
A2
PSB
IO/SEL
U7
LS138
E1
E2A
E2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
INT 3
D0
D1
D2
D3
D4
D5
D6
D7
U3B
LS74
U3A
LS74
C14
39pF
C13
39pF
U5
LS374
U6
LS374
EN
DS13
DS10
DS11
DS9
DS12
DS1
DS3
DS5
DS7
DS8
DS6
DS4
DS2
R39
R36
R37
R35
R38
R27
R29
R31
R33
R34
R32
R30
R28
R40
R41
R42
R43
R44
R45
R46
R48
R49
R50
R51
R52
R53
R54
R55
10K
SW1
SW7
SW8
SW14
SW2
SW9
SW3
SW10
SW4
SW11
SW15
SW5
SW12
SW16
SW17
SW19
SW21
SW23
SW6
SW13
SW18
SW20
SW22
SW24
P2
REFERENCE
A11
P1
C3-C5
C7-C12
0.1
+5V RTN
-15V
+15V
ANG GND
NOTES:
UNLESS OTHERWISE SPECIFIED,
RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS, AND INDUCTANCES ARE IN MICROHENRIES
MATCHING CONNECTIONS FOR SIGNAL FLAGS ARE LOCATED BY SHEET NUMBER AND GRID COORDINATE
DENOTES TEST POINT

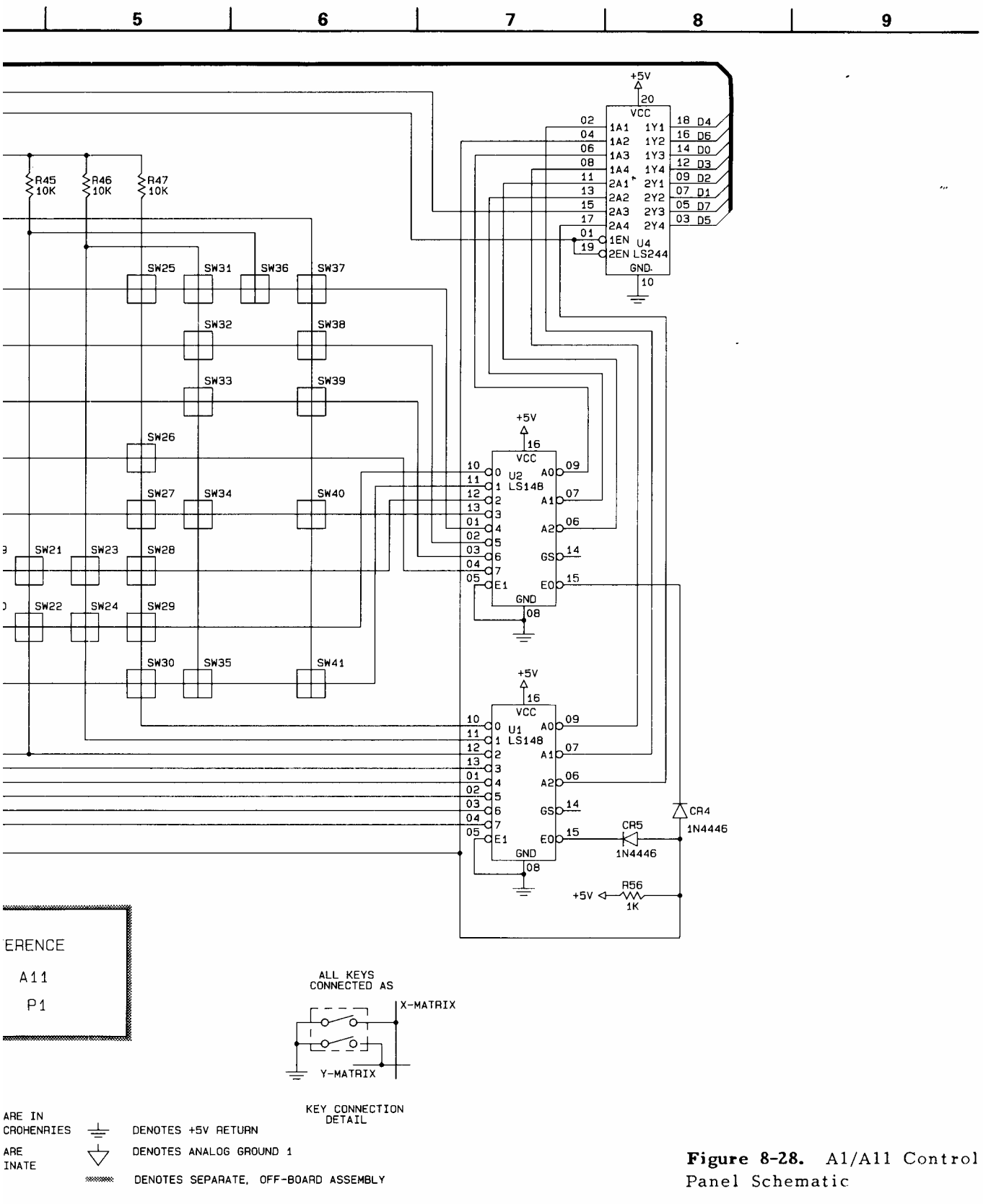
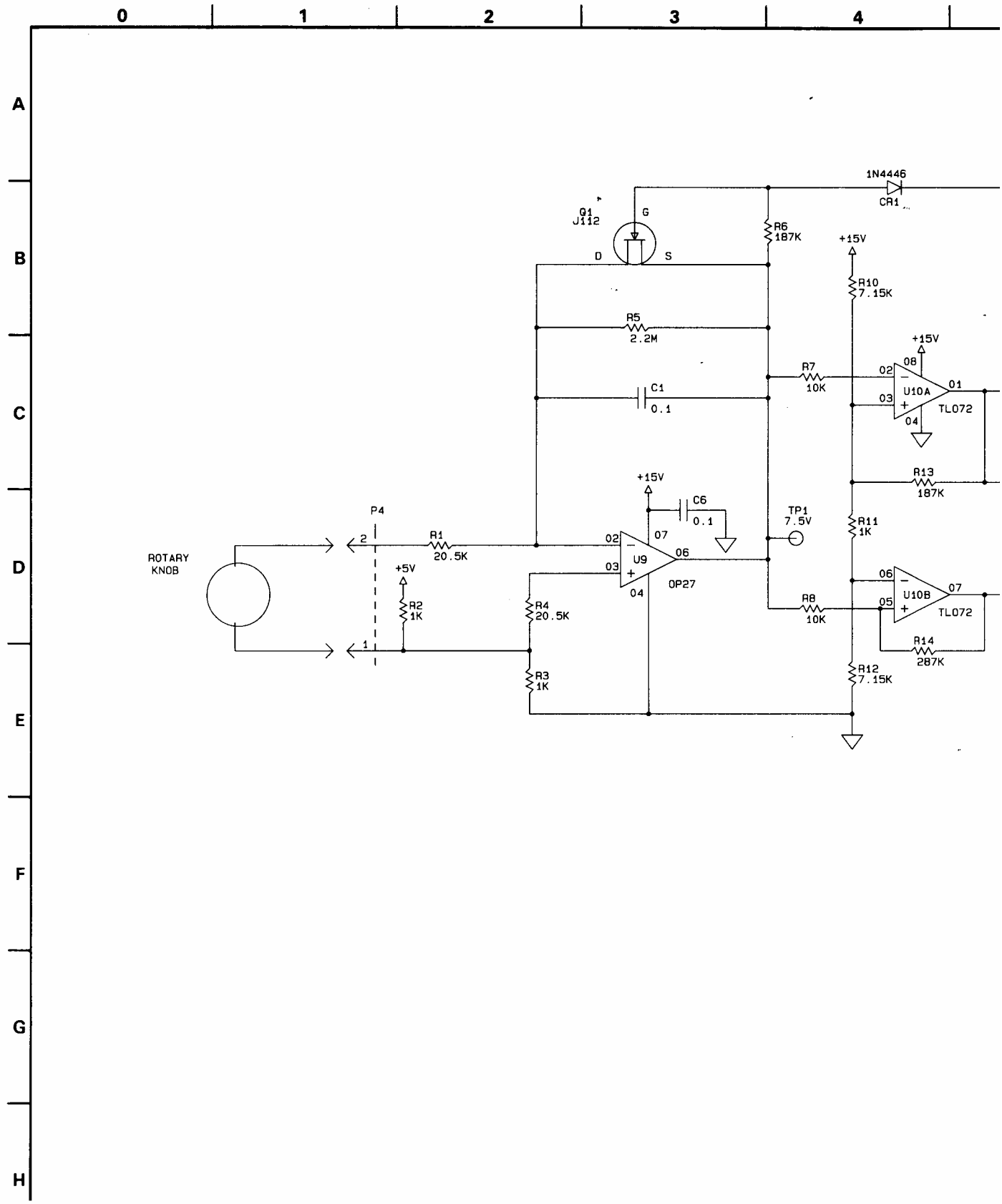


Figure 8-28. A1/A11 Control Panel Schematic


0
1
2
3
4
A
B
C
D
E
F
G
H
1N4446
CR1
Q1
J112
G
D
S
R6
187K
+15V
R10
7.15K
R5
2.2M
C1
0.1
R7
10K
U10A
TL072
08
02
03
04
01
R13
187K
+15V
C6
0.1
TP1
7.5V
R11
1K
P4
2
1
R1
20.5K
ROTARY
KNOB
+5V
R2
1K
R4
20.5K
R3
1K
U9
OP27
07
06
02
03
04
U10B
TL072
06
05
07
R8
10K
R14
287K
R12
7.15K

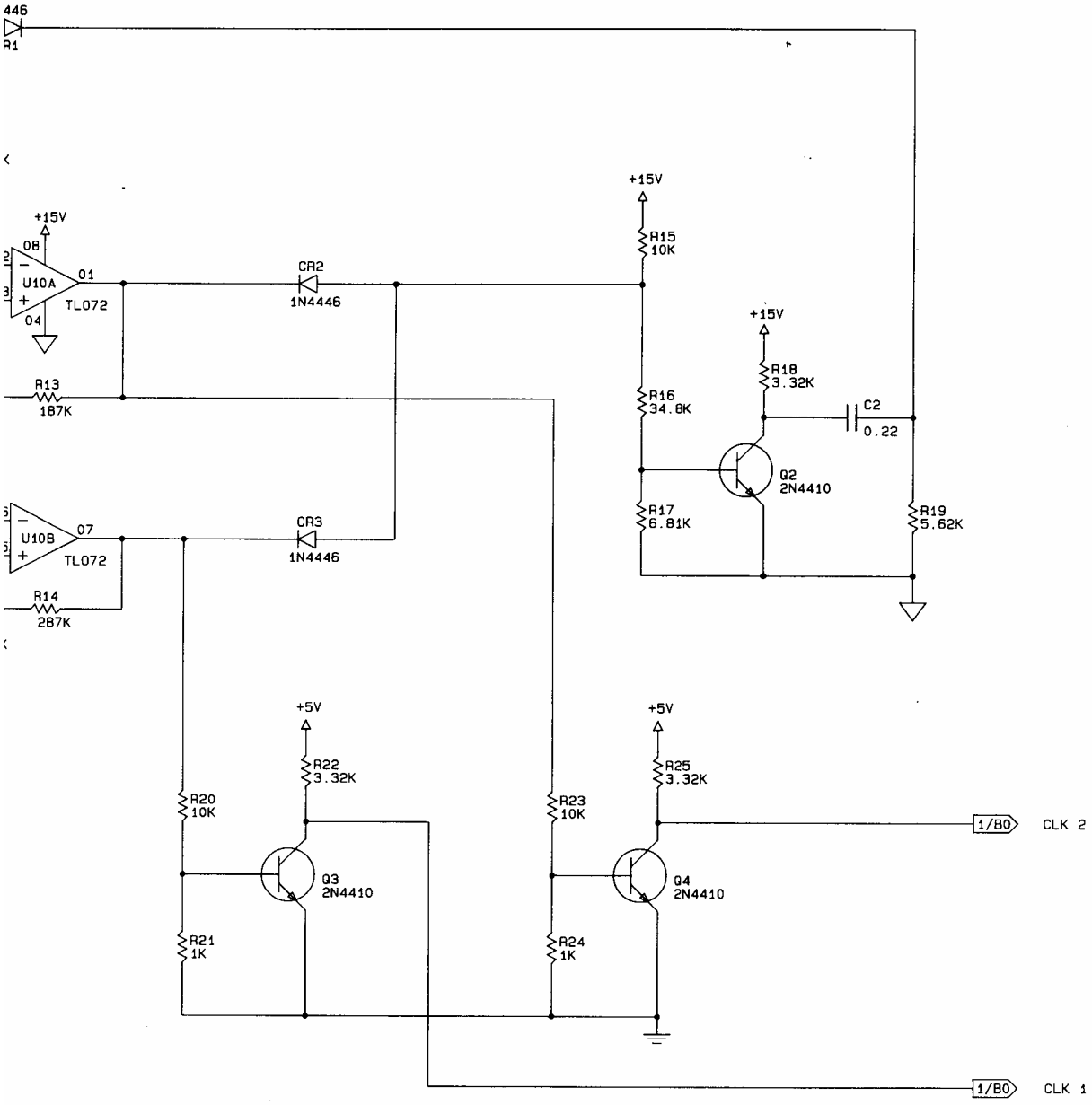


Figure 8-28. A1/A11 Control Panel Schematic (Continued)

8-7.3 A3 Signal Channel PCB

The A3 signal channel PCB provides the interface between the A6 CPU PCB and the measurement components.

The overall circuit block diagram is shown in Figure 8-36. The parts locator diagram and schematic are shown in Figures 8-37 and 8-38. Unless otherwise directed, refer to the overall block diagram (Figure 8-36) for the following discussions.

a. General. The A3 Signal Channel PCB:
   1. Takes the signal from a detector or autotester.
   2. Amplifies it to a suitable level.
   3. Digitizes the signal.
   4. Sends the resultant data in either a linear or logarithmic form over the bus when requested by the CPU (A6).

   The A3 PCB also reads the voltage drop of the thermistor and log conformity resistors contained in the detectors and autotesters so that the CPU can make the necessary corrections for temperature and log conformity. At higher power levels the CPU performs corrections for the actual departure from square law characteristics of the detector diodes.

   Three power supply voltages are supplied to the A3 PCB via the ribbon cable: +5V, +15V, and -15V. The ribbon cable also provides the interface between the A3 PCB and the A6 PCB.

b. Signal Outputs. The detector and autotester signal outputs connected to channels A and B are linked to the A3 Signal Channel PCB through four, core-shielded cables. Channel A is connected to connector P1 and channel B is connected to Connector P2. These connections are as follows:

Front Panel Connector	Function	Signal Channel Connector
Pin 1	Det. Line	Pin 1
Pin 2	Det. Return	Pin 2
Pin 5	Det. Shield	Pin 3
Pin 3	Det. Log	Pin 4
Pin 4	Det. Therm.	Pin 5

The appropriate channel to be read is switched through a two-way multiplexer (MUX) to a three stage linear dc amplifier. The output of a detector can vary from -0.5μV to -2.0V (approximately), depending on applied RF power. Hence, optimum amplifier gain can be selected under CPU control while preventing output saturation.

Field Effect Transistors (FETs) Q1, Q6, Q2, and Q7 form the input multiplexer: Q1 and Q6 are turned on simultaneously to select channel A, while Q2 and Q7 are turned on simultaneously to select channel B. Quad operational amplifiers U27A and U27B drive the FETs.

c. Instrumentation Amplifier. The multiplexed channel signal is applied to the differential inputs of U1, an instrumentation amplifier. U1 is also a programmable gain amplifier that can be switched between 4 decade gains: unity, x10, x100, and x1000. VMOS FETs Q3, Q4, and Q5 (Figure 8-29), the switching elements that set the gain of U1, are driven by three sections of the quad operational amplifier, U28. The gain is selected as follows:

GAIN	ON	OFF
1		Q3, 4, 5
10	Q3	Q4, 5
100	Q4	Q3, 5
1000	Q5	Q3, 4

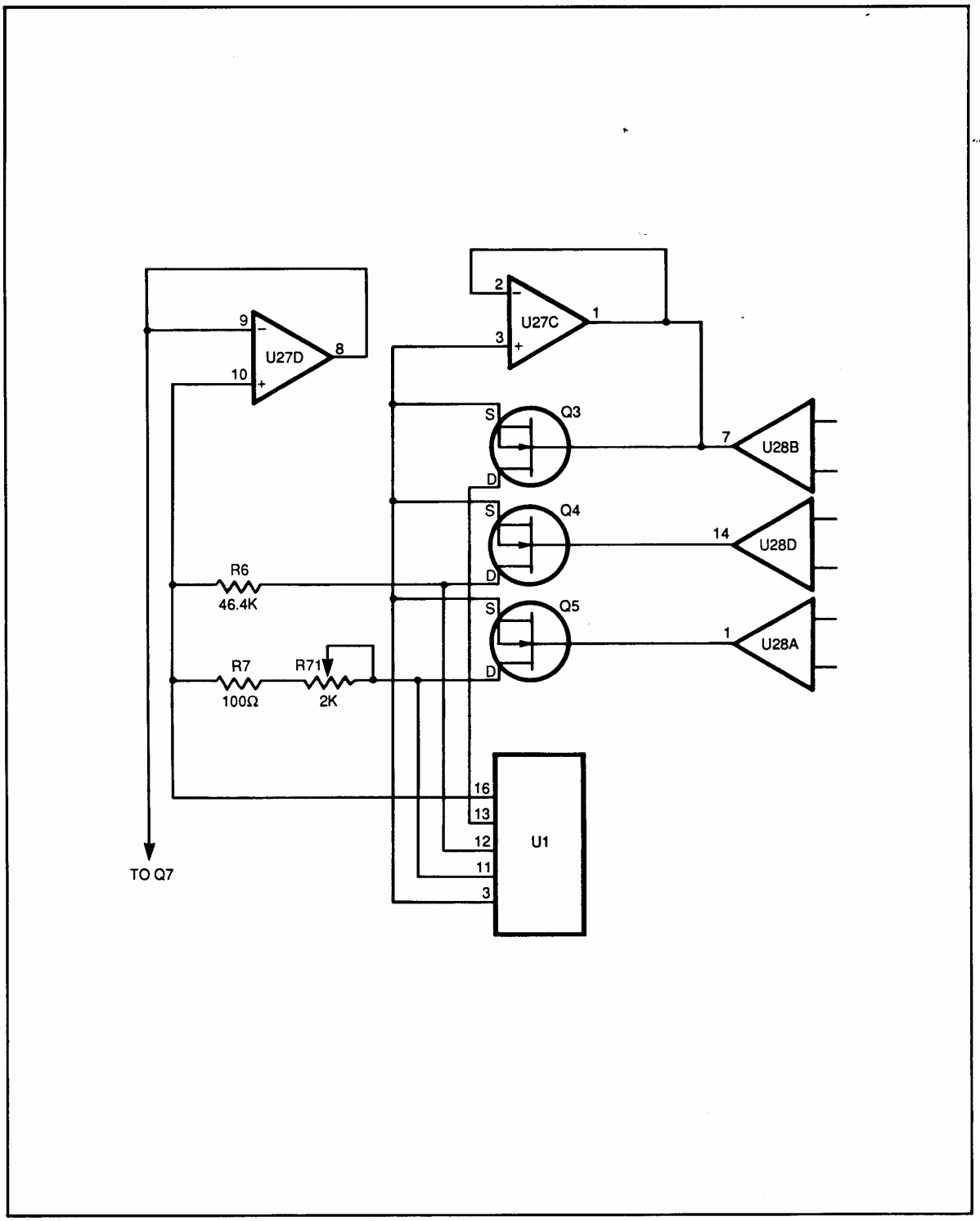


Figure 8-29. Instrumentation Amplifier, 1st stage

Preset potentiometer R71 precisely trims the gain of U1 when U1 is switched to the gain of 1000 position. The two remaining sections of U27 (C and D) are connected as followers to hold the gates of the input MUX and gain switching FETs to within approximately 0.65V when in the switched-ON condition.

The next two stages of the linear amplifier (Figure 8-30) consist of FET operational amplifiers U2 and U3. U2, a non-inverting operational amplifier stage, can be switched between a gain of unity and x100 by quad FET switches U23A and U23B. Preset potentiometer R34 provides a means of precisely setting the x100 gain. High frequency roll off of the amplifier's gain is provided by C7 in combination with the feedback resistance of R34 in series with R35.

The U3 amplifier stage is similar to that of U2 except that its gain is switchable between a gain of x5 and x50 by the two remaining sections of U23, C and D.

The actual overall gain is trimmed to approximately x1 and x10 by the preset potentiometer R38 in the potential divider chain, R36, R37, and R38. This preset provides for overall trimming of the signal channel gain during final calibration of the instrument.

Although the gain of the U3 stage is changed by this process, the ratio between its fixed gains remains at 10:1. This ratio can be trimmed exactly using preset potentiometer R42. High frequency roll off of the stage is provided by C8 and C9. The two preset potentiometers, R29 and R31, allow trimming of the operational amplifiers output stages to compensate for input offset voltages.

c. Autozero. The autozero mechanism compensates for the offset voltages from the output of the three stage amplifier. These offset voltages occur due to changes of time, temperature, and device characteristics.

Two autozero circuits are actually provided because some of the offset voltages occur due to an offset generated by the detector or autotester connected to the channel. The autozero circuits are switched together with the input multiplexing FETs: Q1, Q6, Q2, and Q7. This switching applies an offset compensation voltage to the input of the ampifier chain at U1. Hence, the offset voltage is reduced to zero when there is no applied RF at the detector or autotester.

d. Integrating Circuits. An integrating circuit is the basis of each autozero circuit. The following discussion describes only the Channel A zeroing action since both integrating circuits are identical. Figure 8-31 shows the essential elements of this circuitry.

U14, a FET operational amplifier, is connected as the integrator that zeroes channel A. The time constant of this integrator is normally set by C11 and R46. If, however, the output of the linear amplifier chain is greater than approximately + or -10V, zener diodes CR11 and CR12 conduct, and the time constant is then set by C11 and R45. Since the value of R45 is much smaller than R46, the zeroing circuit acts more rapidly to zero the amplifier in a saturated situation.

To zero the signal channel's linear amplifier when it is connected to channel A, the CPU waits until the end of a screen trace, then turns the instrument's source RF OFF. Thus, if the detector or autotester is connected to a device under test, no RF is present. Any small amount of RF leakage that is present is dealt with as a dc offset by the autozero circuit.

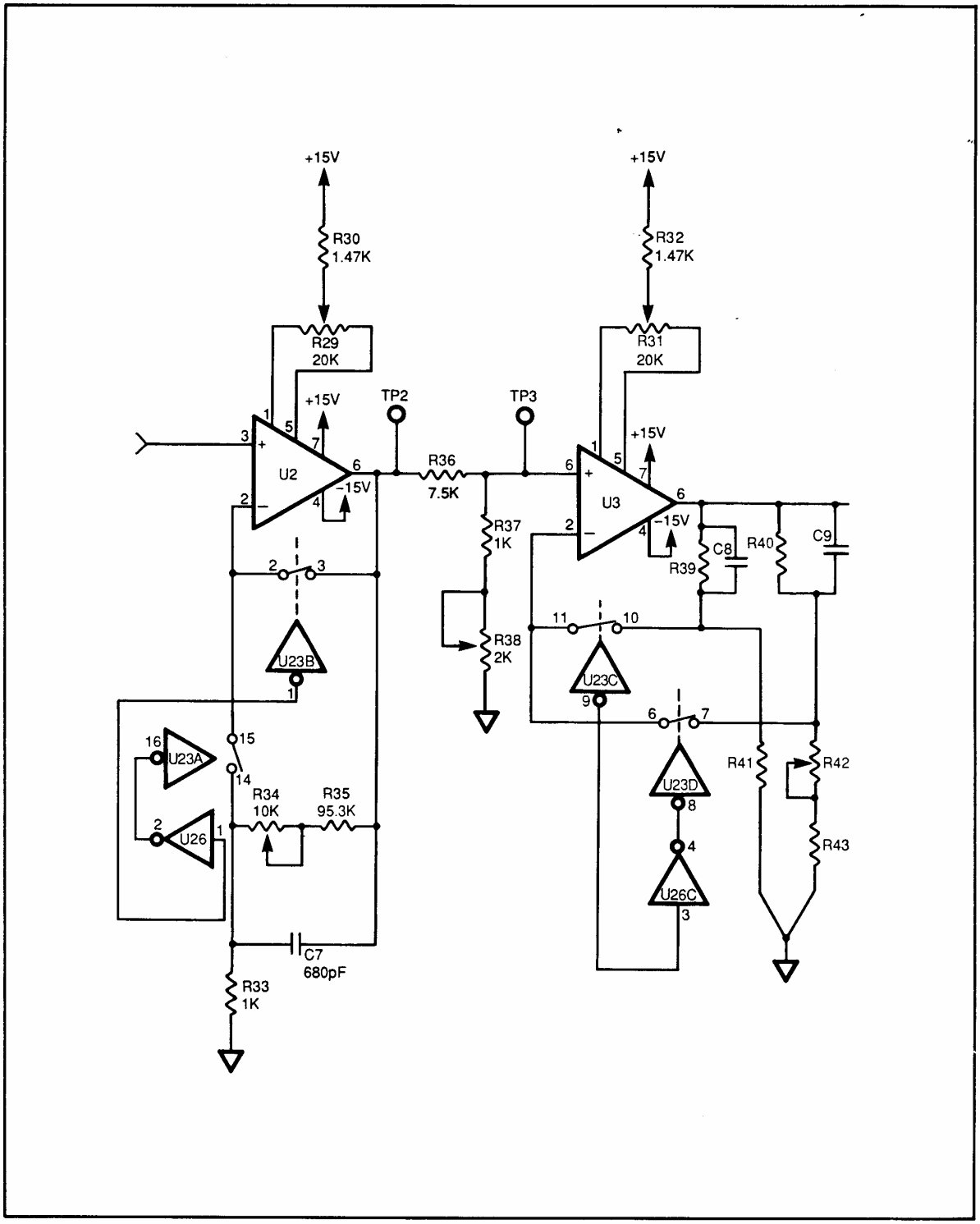


Figure 8-30. Instrumentation Amplifier, 2nd and 3rd stages

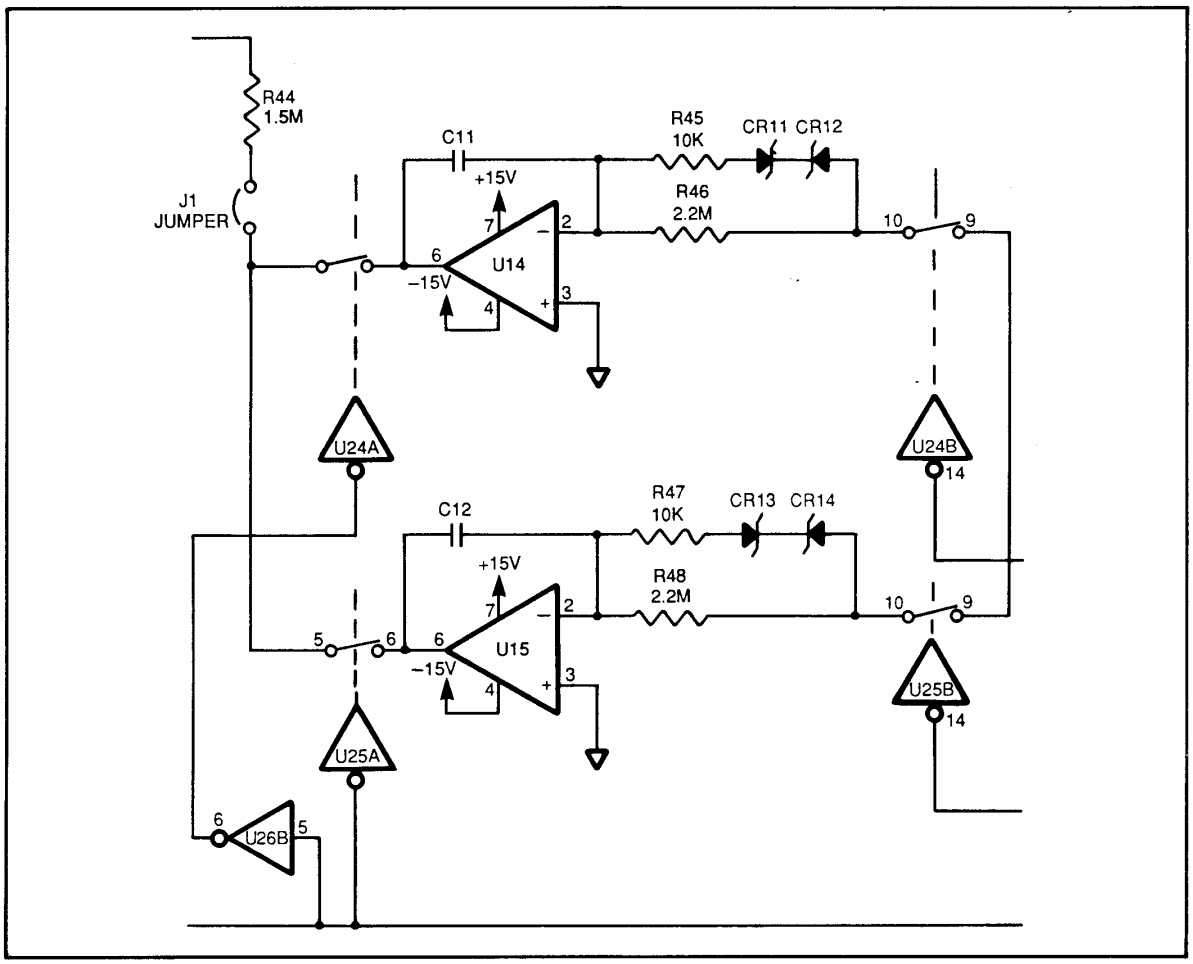


Figure 8-31. Integrating Circuitry

When the RF has settled to OFF, the CPU sets the gain of the linear amplifier chain to maximum. The CPU then operates the dual FET switch, U24, so that the switch element at both the input and output of the integrator is ON. The two switch elements in the channel B autozero circuit, U25, are switched to OFF.

If, for example, there is a positive offset voltage present at the output of the amplifier chain, the integrator capacitor C11 begins to charge. As C11 charges, the output of the integrator moves in a negative direction.

The operation is similar for a negative offset voltage, except that all polarities are reversed. This negative voltage is applied to the offset null pins (pins 4 and 5) of U1. The negative voltage reduces the amount of offset present.

The integrator eventually charges to a level great enough to bring the amplifier chain output offset voltage to zero. If the switch at the integrator input is then opened, the integrator output will remain at this level for a long period without significant change. Any eventual drift is caused by internal leakage

within the circuit. Since C11 is a low value capacitor, leakage is very small.

When the source RF is turned back ON by the processor, the linear amplifier chain responds to the RF in the normal way, except that compensation has been made for offset voltage error. To compensate for drift, zeroing action occurs at the end of every sweep.

When the 6400 is switched ON, or when a detector or autotester is changed, the amplifier may experience a particularly large offset voltage. If this is the case, the zeroing action may take several sweeps to complete the zeroing process.

Channel B autozeroing action takes place similarly through U15. If both channels A and B are selected from the instrument control panel, the CPU will sweep out first one channel trace and then the next, alternately. The zeroing action for each channel occurs at the end of that channel's sweep.

e. Smoothing. The smoothing function provides a stable, jitter-free CRT display. The smoothing circuitry is shown in Figure 8-32.

The output of the linear amplifier then passes through a switched, passive, CR filter network. This network is made up of R57 and one or none of capacitors C3, C4, C5, and C6, as selected by the quad FET switch, U22. When no smoothing is selected from the instrument control panel, no smoothing capacitance is switched in. And, the frequency response is that set by the preceding linear amplifier stages. If minimum smoothing is selected, capacitors C5 and C6 provide the extra filtering for Channel A and Channel B, respectively. If maximum smoothing is selected, the extra smoothing is provided by capacitors C3 and C4 for Channel A and Channel B respectively.

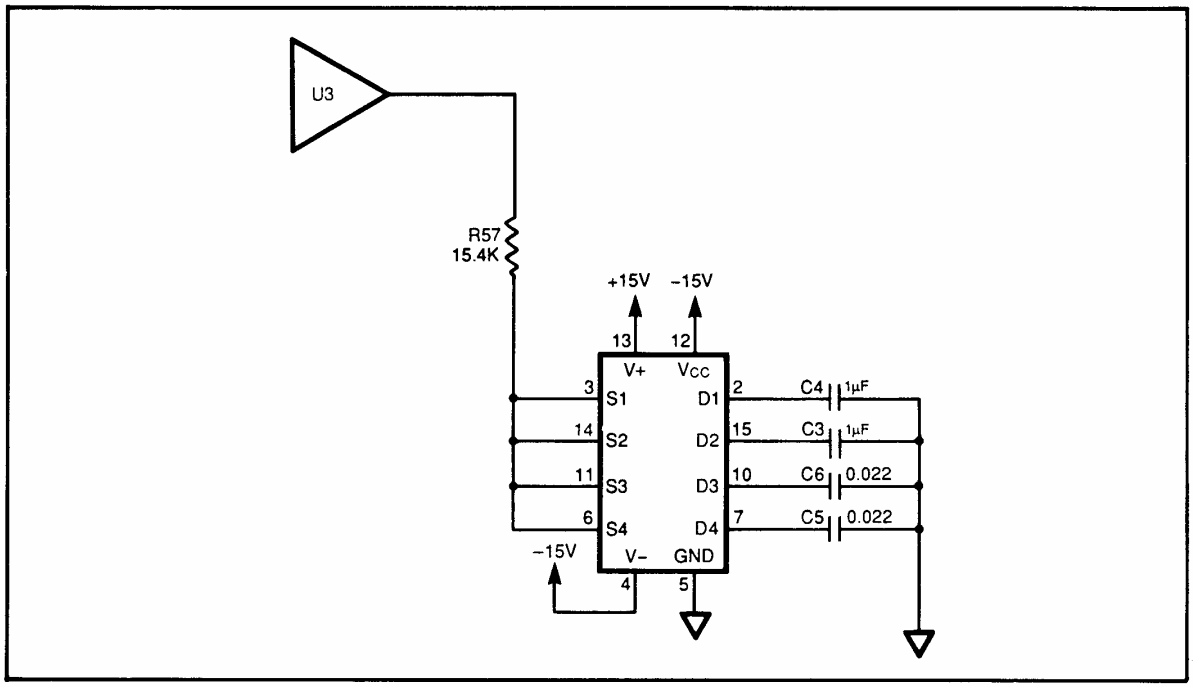


Figure 8-32. Smoothing Circuitry

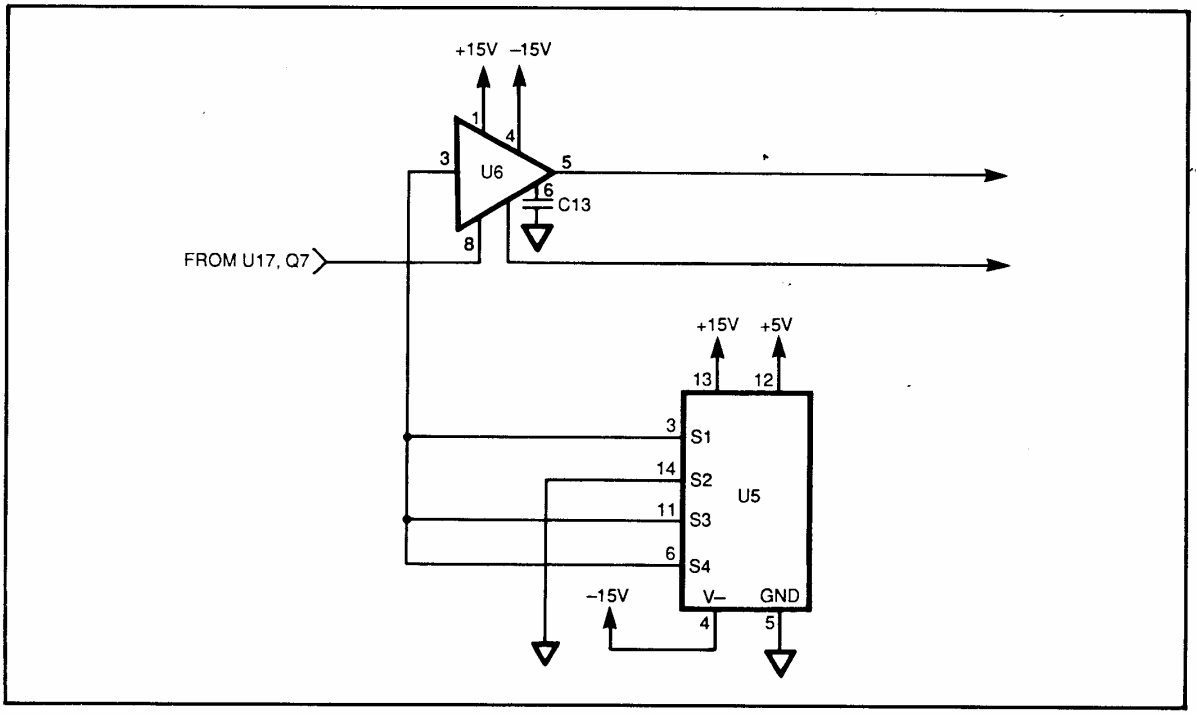


Figure 8-33. Sample and Hold Circuitry

The speed of the instrument sweep is automatically slowed to an appropriate rate by the CPU. This allows for the greater settling time of the signal channel. The user, therefore, need not adjust the sweep speed when using the smoothing function of the instrument.

f. Sample and Hold. The output of the smoothing filter circuit is connected to the sample and hold amplifier, U6 (Figure 8-33), through a two way multiplexer, U5. This multiplexer is a FET switch circuit, switching between reading the output of the linear amplifier and reading the detector/autotester thermistor and log conformity resistors.

If, for example, U5 is switched to read the output of the linear amplifier, the CPU switches U6 to hold. The CPU then reads the voltage of capacitor C13, the hold capacitor. The voltage held at the output of U6 will be negative since the output of a WILTRON detector is negative and the signal channel linear amplifier is non-inverting. Before the held voltage can be converted, however, it must pass through U7, the level-shifting/inverting stage.

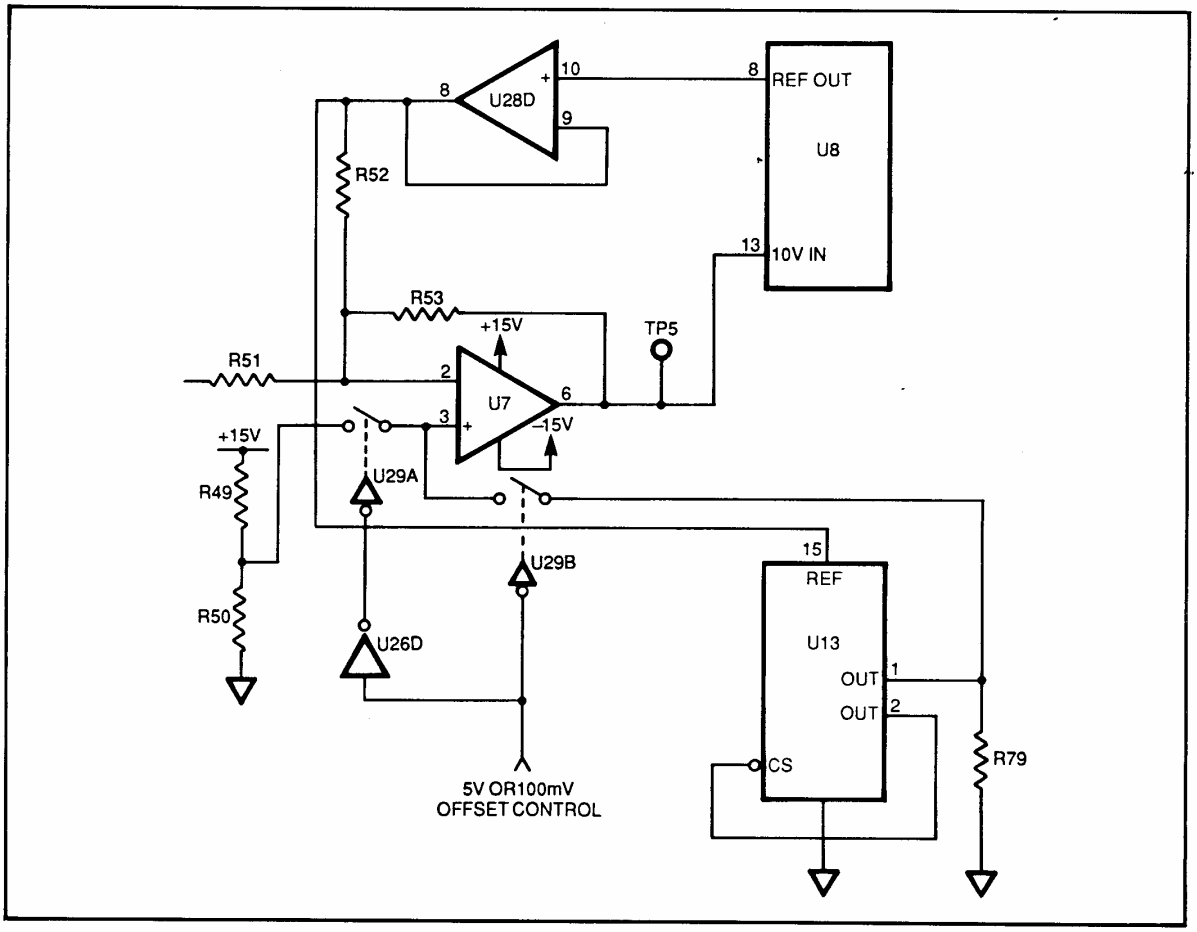


Figure 8-34. Level-Shifting/Inverting Stage

g. Level-Shifting/Inverting. The level-shifting/inverting stage, U7, performs three functions:

1. It inverts the applied signal so that it is positive when input to the U8 ADC (Figure 8-34).
2. It provides a way for the CPU to null offsets using the U13 DAC. These offsets are caused by two factors because:
   (a) The signal channel autozero only takes place with the linear amplifier switched to maximum gain.
   (b) Small differences in zero may occur when it changes range during a sweep.
3. It permits an offset of +5V to be applied to the voltage being read by the CPU.

   This +5V application places noisy signals, such as those that occur on the higher gain ranges of the signal channel, within the input range of the ADC. Otherwise, the negative going excursions of the noisy signal would be clipped when read by the ADC. Subsequently, signal processing by the CPU would be biased in a positive direction.

When the 6400 is switched ON or when self test or reset is requested, the CPU performs an autozero. The CPU then switches through all ranges of the three stage linear amplifier, measuring the amount of residual offset voltage present for each range. This is done for both channels.

The offset voltage values are stored by the CPU. The CPU uses the values to apply an appropriate offset correction voltage, through U13, for each range as it is used during instrument operation. The output of the level shifting stage can be offset by plus or minus 100mV, allowing correction of residual offsets in the range of plus and minus 100mV.

h. ADC. ADC (analogue to digital converter) U8 is unipolar in operation, and converts inputs in the range 0 to +10V.

U8 is a 12 bit device that obtains its +5V supply from U21, a low-power, voltage regulator fed from the +15V supply. This arrangement provides extra decoupling by isolating the sensitive analogue circuitry from the potentially noisy +5V digital supply.

The U8 ADC has its own on-chip voltage reference. This reference is externally buffered by U28D (Figure 8-34) and used as a reference to the level-shifting/inverting stage, U7, to the U13 DAC.

After the signal has been converted by the ADC, the digital representation of the amplified detector/autotester output voltage can be read by the CPU. The CPU can read the voltage in two ways:

1. As linear data, in which case the 12 bit output of the ADC is read directly over the bus in two bytes via tri-state buffers U11 and U12 (Figure 8-36).
2. Or, as a two byte logarithmic representation of the ADC data that is obtained by addressing the U9 Log PROM (programmable read only memory) with the ADC data.

This Log PROM contains a logarithmic look-up table. The logarithmic data output is read over the bus via tri-state buffer U10.

i. PROM Table. Performing the logarithmic conversion digitally avoids the potential error caused by the drift of a conventional logarithmic amplifier. The look-up PROM table contains data to cope with a 12 dB change in signal level, which is why the signal channel switches gain in decade ranges.

For example, assume the applied signal is at the top of the log PROM table for a given power applied to a detector. If this applied power falls by 10 dB, the signal at the log PROM falls to a tenth of its full scale reading and the log PROM goes 10 dB down in its look-up table.

If the applied power continues to fall, the signal channel linear amplifier increases its gain by a factor of ten and goes back to the top of the log PROM data table. The 12 dB of log table allows for some overlap between gain ranges, which provides hysteresis. This prevents gain-change oscillations when the applied signal falls on the border of two adjacent ranges.

Data read via the Log PROM works well for relatively high levels of detected RF. However, when measuring low-level, noisy signals, the 6400 reads data linearly so that it can be manipulated by the CPU. The CPU uses the +5V offset facility and a logarithm generating algorithm to accurately extract the required data from the noise level.

Linearly read data is also necessary when the CPU wants to:

1. Measure the residual offset of the linear amplifier.
2. Read the thermistor and log conformity resistors.

j. Log Conformity and Thermistor Signals. The log conformity and thermistor signals are read by switching the two way multiplexer, U5, from the output of the linear amplifier to the output of the four way multiplexer, U4.

Channel A thermistor, Channel A log conformity, Channel B thermistor and Channel B log conformity resistors contained in the detector/autotesters are connected to the circuit to complete the potential dividers formed across the four inputs of U4.

Changes in these resistor values are read as changes in voltage through the digitizing function of the signal channel performed by U6 and U8. Preset potentiometers R76 (Channel A adjustment) and R77 (Channel B adjustment) (Figure 8-35) are included in the A and B log conformity potential dividers to achieve the required accuracy in the log conformity case.

Besides going to the four way multiplexer inputs of U4, the output of each log conformity potential divider goes to comparator U30A and U30B. The output of U30 is read over the bus as spare bits on the second linear data byte from the U8 ADC. Also included on this data byte is the status signal of the U8 ADC. This signal tells the CPU when the U8 ADC has finished its conversion.

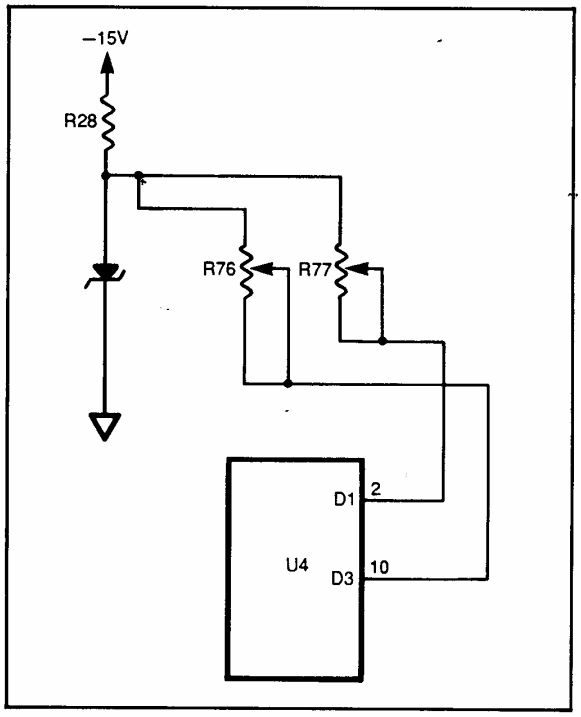


Figure 8-35. Preset Pots R76 and R77

If a detector or autotester is connected to the 6400, the output of the U4 comparator will be HIGH. This HIGH output indicates to the CPU that the detector or autotester is present. If no detector or autotester is present, the output of the U4 comparator will be LOW. This LOW output is read by the CPU as a logic 0. Thus, the CPU does not try to zero a channel which has its input disconnected.

Digital control of the signal channel functions described thus far is achieved by decoding CPU commands sent over the bus. This decoding uses the two three-to-eight line decoder ICs, U18 and U19. The commands are decoded as shown in Table 8-8.

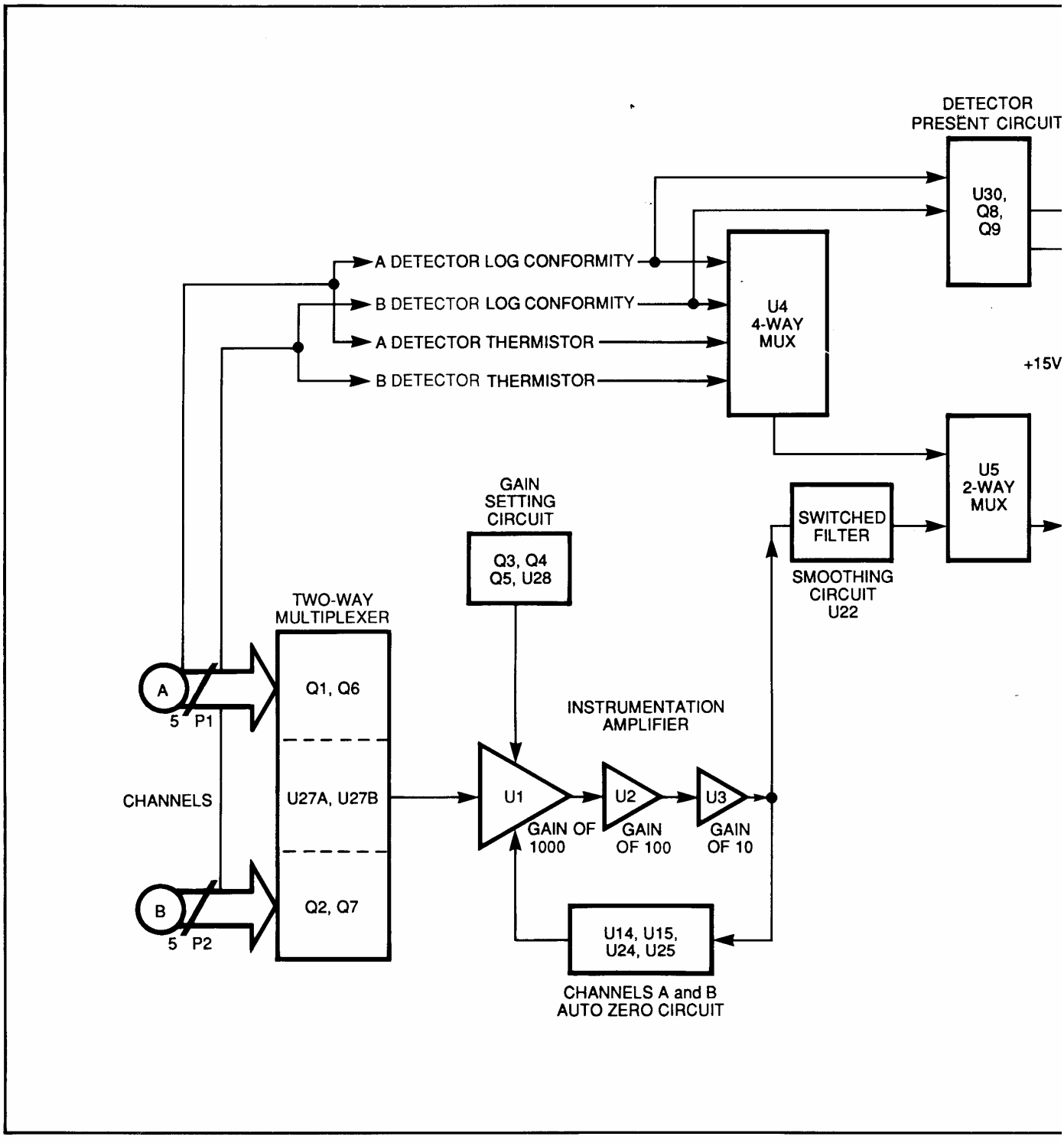
Table 8-8. Decoding CPU Commands

Port#	IC#	PIN#	Function
08	U18	15	Enable U12, 2nd byte of ADC data
09	U18	14	Enable U11, 1st byte of ADC data
0A	U18	13	Write data to latch U17
0B	U18	12	Write data to latch U16
0D	U18	10	Write data to latch U20
10	U19	15	Start ADC conversion
12	U19	14	Read logarithmic data word
16	U19	12	Write data to null DAC U13

Data is written/read using octal latches and octal tri-state buffers. The data to octal latches U16, U17, and U20 can be written as shown in Table 8-9.

Table 8-9. Octal Latch Data

Octal Latch U16	
Data Bit	Function
D7	A channel, min. filtering
D6	B channel, min. filtering
D5	B channel, max. filtering
D4	A channel, max. filtering
D3	No connection
D2	Set U5 to read linear amp.
D1	Set U5 to read thermistor/log conformity MUX.
D0	Ground DET RETURN when reading thermistor/log conformity MUX.
Octal Latch, U17	
Data Bit	Function
D7	Select B channel log conformity
D6	Select A channel log conformity
D5	Select A channel thermistor
D4	Select B channel thermistor
D3	No connection
D2	No connection
D1	Sample/hold
D0	5V/DAC offset
Octal Latch, U20	
Data Bit	Function
D7	Select U1 gain of 1000
D6	Select U1 gain of 100
D5	Select U1 gain of 10
D4	Select U2 gain of 100/1
D3	Select U2 gain of 10/1
D2	Channel A autozero
D1	Channel B autozero
D0	Channel A/B input multiplexing


DETECTOR
PRESENT CIRCUIT
U30,
Q8,
Q9
A DETECTOR LOG CONFORMITY
B DETECTOR LOG CONFORMITY
A DETECTOR THERMISTOR
B DETECTOR THERMISTOR
U4
4-WAY
MUX
+15V
U5
2-WAY
MUX
SWITCHED
FILTER
SMOOTHING
CIRCUIT
U22
GAIN
SETTING
CIRCUIT
Q3, Q4
Q5, U28
TWO-WAY
MULTIPLEXER
A
5
P1
Q1, Q6
CHANNELS
U27A, U27B
B
5
P2
Q2, Q7
INSTRUMENTATION
AMPLIFIER
U1
GAIN OF
1000
U2
GAIN
OF 100
U3
GAIN
OF 10
U14, U15,
U24, U25
CHANNELS A and B
AUTO ZERO CIRCUIT

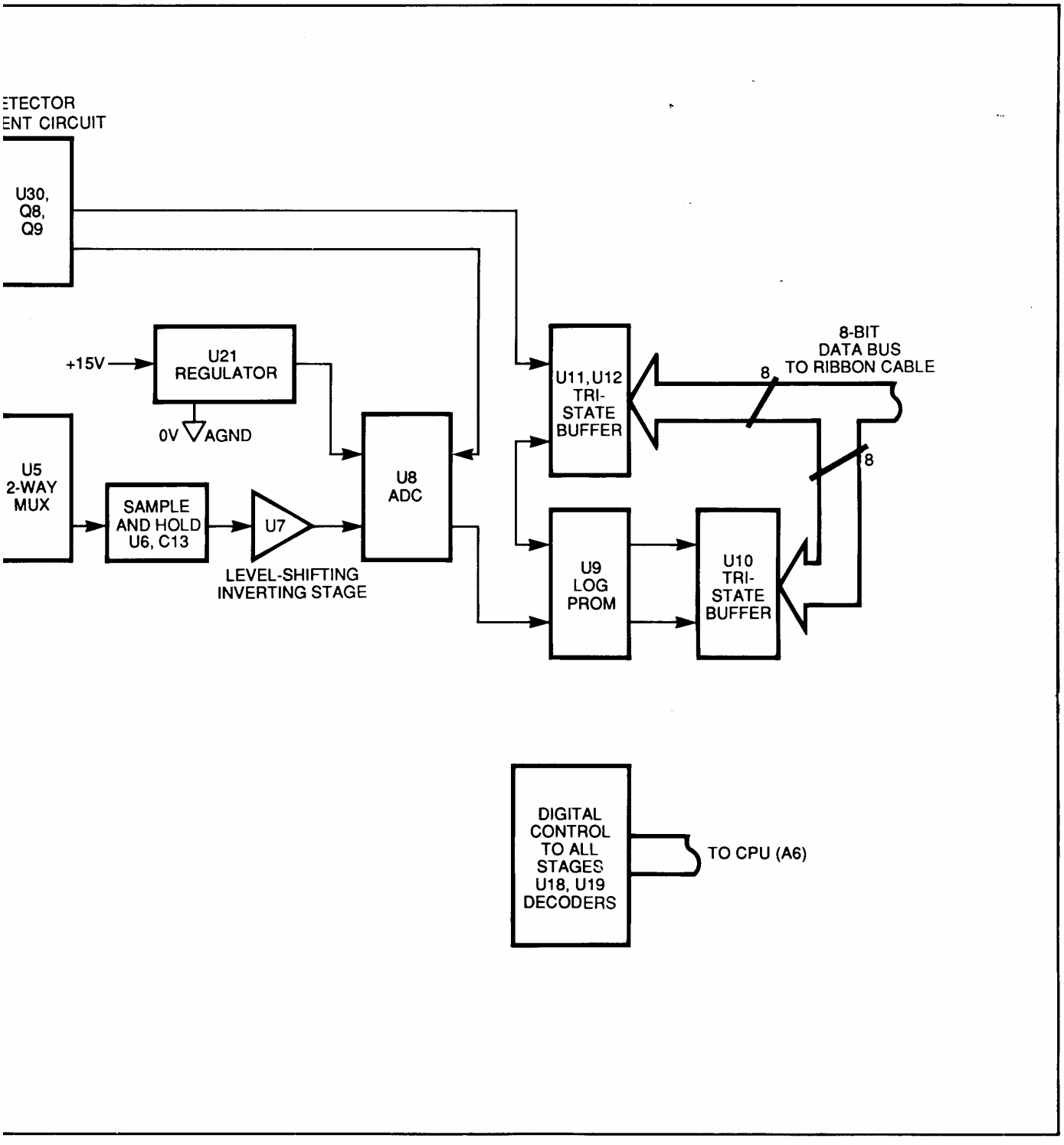


Figure 8-36. A3 Signal Channel Block Diagram

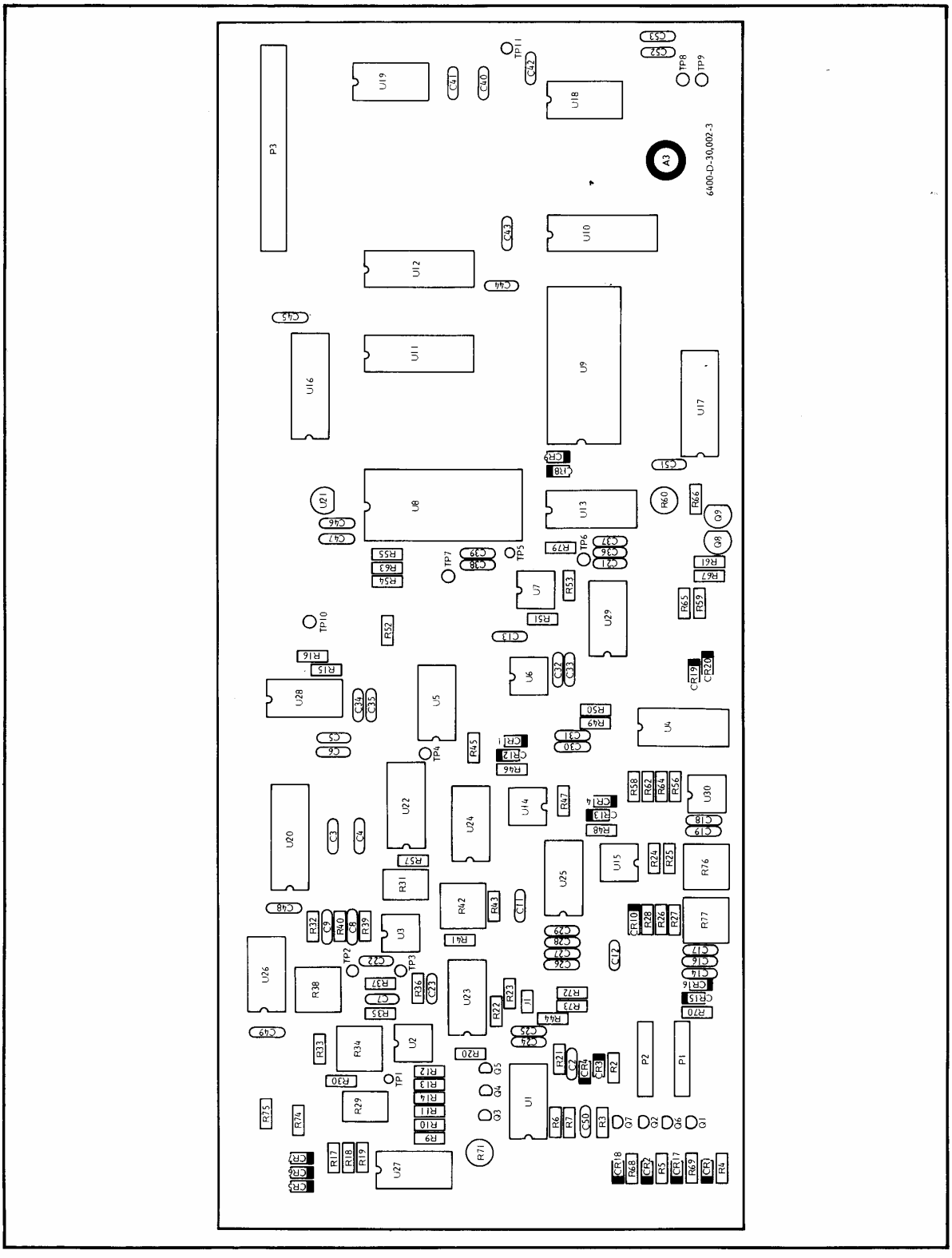
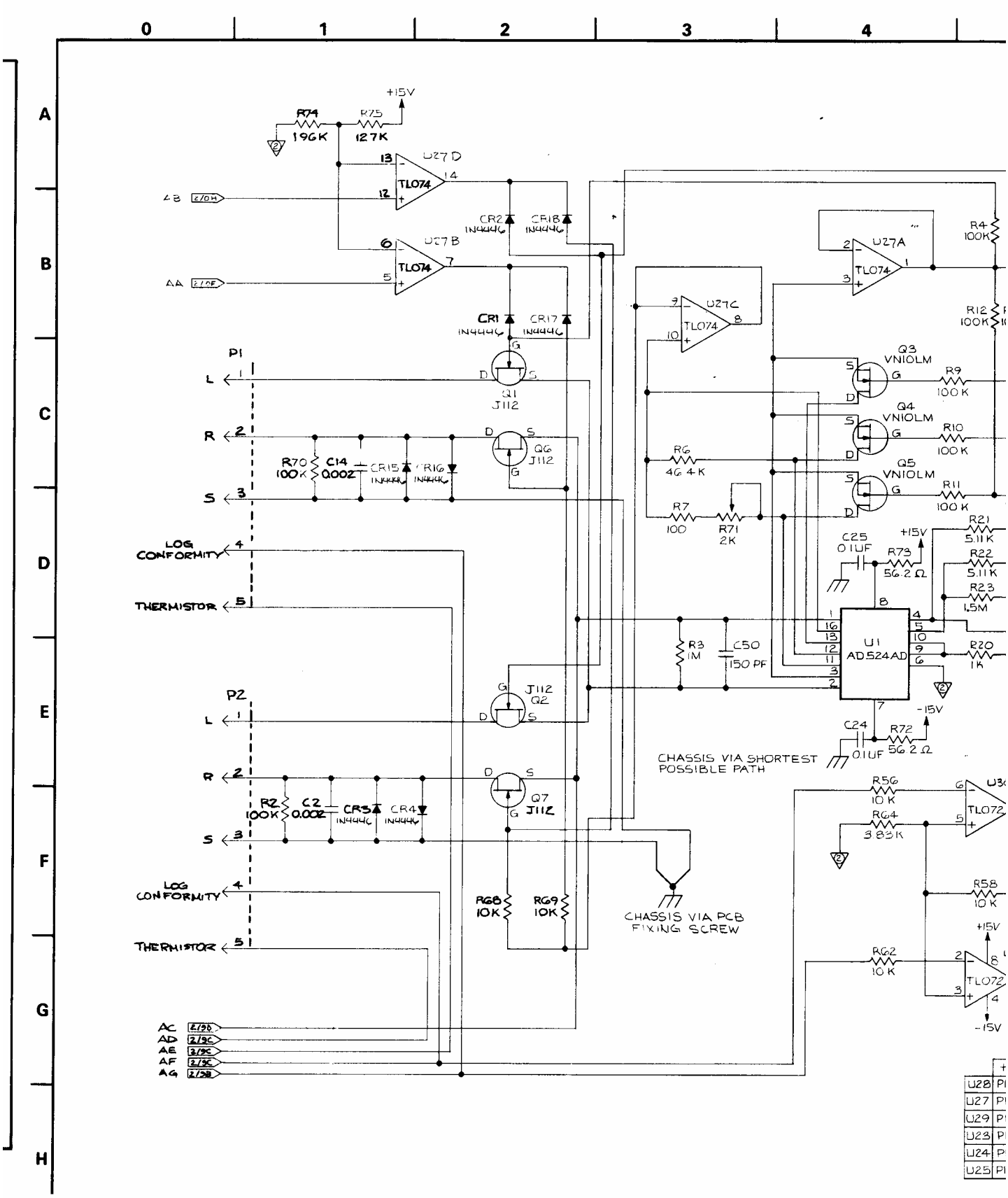
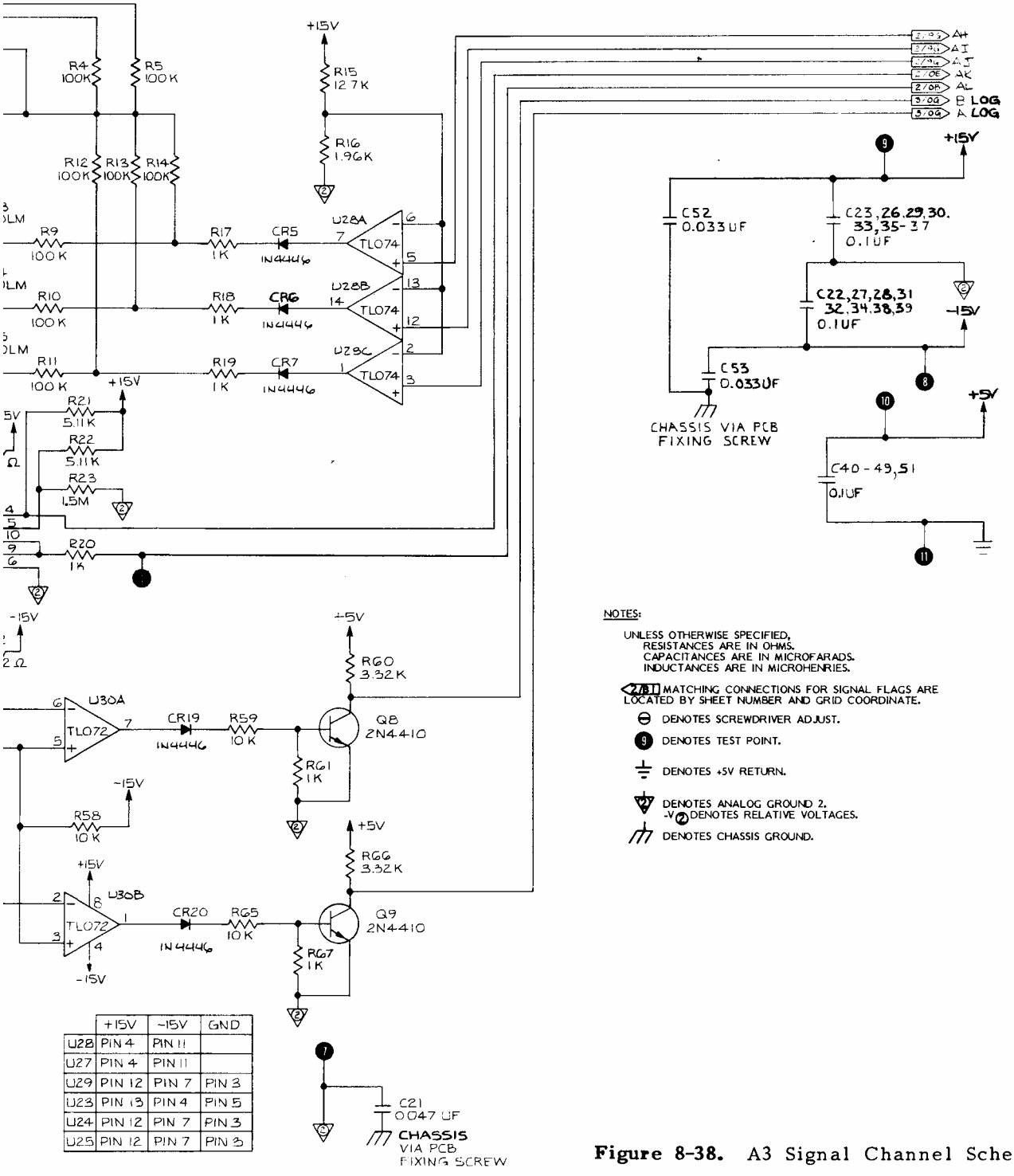


Figure 8-37. A3 PCB Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
+15V
R74
196K
R75
127K
U27D
TLO74
U27B
TLO74
CR2
IN4446
CR18
IN4446
CR1
IN4446
CR17
IN4446
U27A
TLO74
U27C
TLO74
R4
100K
R12
100K
P1
L
R
S
LOG CONFORMITY
THERMISTOR
Q1
J112
Q6
J112
R70
100K
C14
0.002
CR15
CR16
Q3
VN10LM
Q4
VN10LM
Q5
VN10LM
R9
100K
R10
100K
R11
100K
R6
46.4K
R7
100
R71
2K
C25
0.1UF
R73
56.2Ω
R21
5.11K
R22
5.11K
R23
1.5M
R20
1K
R3
1M
C50
150 PF
U1
AD524AD
-15V
C24
0.1UF
R72
56.2Ω
CHASSIS VIA SHORTEST POSSIBLE PATH
P2
L
R
S
LOG CONFORMITY
THERMISTOR
J112
Q2
Q7
J112
R2
100K
C2
0.002
CR3
IN4446
CR4
IN4446
RG8
10K
RG9
10K
CHASSIS VIA PCB FIXING SCREW
R56
10K
R64
3.83K
TLO72
R58
10K
RG2
10K
TLO72
AC
AD
AE
AF
AG
U28
U27
U29
U23
U24
U25



	+15V	-15V	GND
U28	PIN 4	PIN 11	
U27	PIN 4	PIN 11	
U29	PIN 12	PIN 7	PIN 3
U23	PIN 13	PIN 4	PIN 5
U24	PIN 12	PIN 7	PIN 3
U25	PIN 12	PIN 7	PIN 3

NOTES:

UNLESS OTHERWISE SPECIFIED,
RESISTANCES ARE IN OHMS.
CAPACITANCES ARE IN MICROFARADS.
INDUCTANCES ARE IN MICROHENRIES.

2/B1 MATCHING CONNECTIONS FOR SIGNAL FLAGS ARE LOCATED BY SHEET NUMBER AND GRID COORDINATE.

⊖ DENOTES SCREWDRIVER ADJUST.

9 DENOTES TEST POINT.

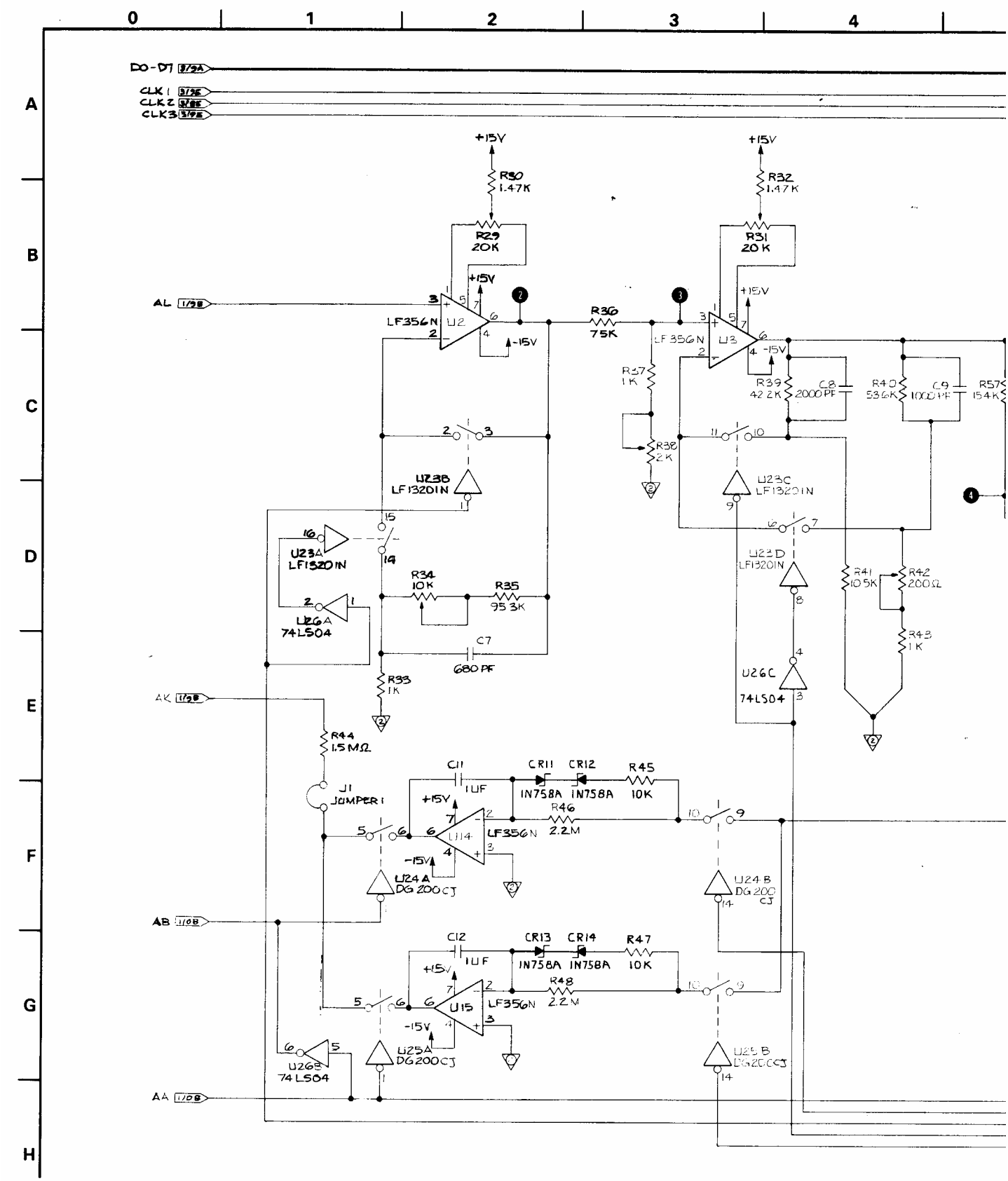
DENOTES +5V RETURN.

DENOTES ANALOG GROUND 2.

-V (2) DENOTES RELATIVE VOLTAGES.

DENOTES CHASSIS GROUND.

Figure 8-38. A3 Signal Channel Schematic


0
1
2
3
4
A
B
C
D
E
F
G
H
D0-D7
CLK1
CLK2
CLK3
AL
AK
AB
AA
+15V
-15V
R30 1.47K
R29 20K
R32 1.47K
R31 20K
U2 LF356N
U3 LF356N
R36 75K
R37 1K
R38 2K
R39 42.2K
C8 2000PF
R40 536K
C9 1000PF
R57 154K
U23B LF1320IN
U23C LF1320IN
U23D LF1320IN
U23A LF1320IN
U26A 74LS04
U26C 74LS04
U26B 74LS04
R34 10K
R35 953K
C7 680PF
R33 1K
R41 105K
R42 200Ω
R43 1K
R44 1.5MΩ
J1 JUMPER
C11 1UF
CR11 IN758A
CR12 IN758A
R45 10K
U14 LF356N
R46 2.2M
U24A DG200CJ
U24B DG200CJ
C12 1UF
CR13 IN758A
CR14 IN758A
R47 10K
U15 LF356N
R48 2.2M
U25A DG200CJ
U25B DG200CJ

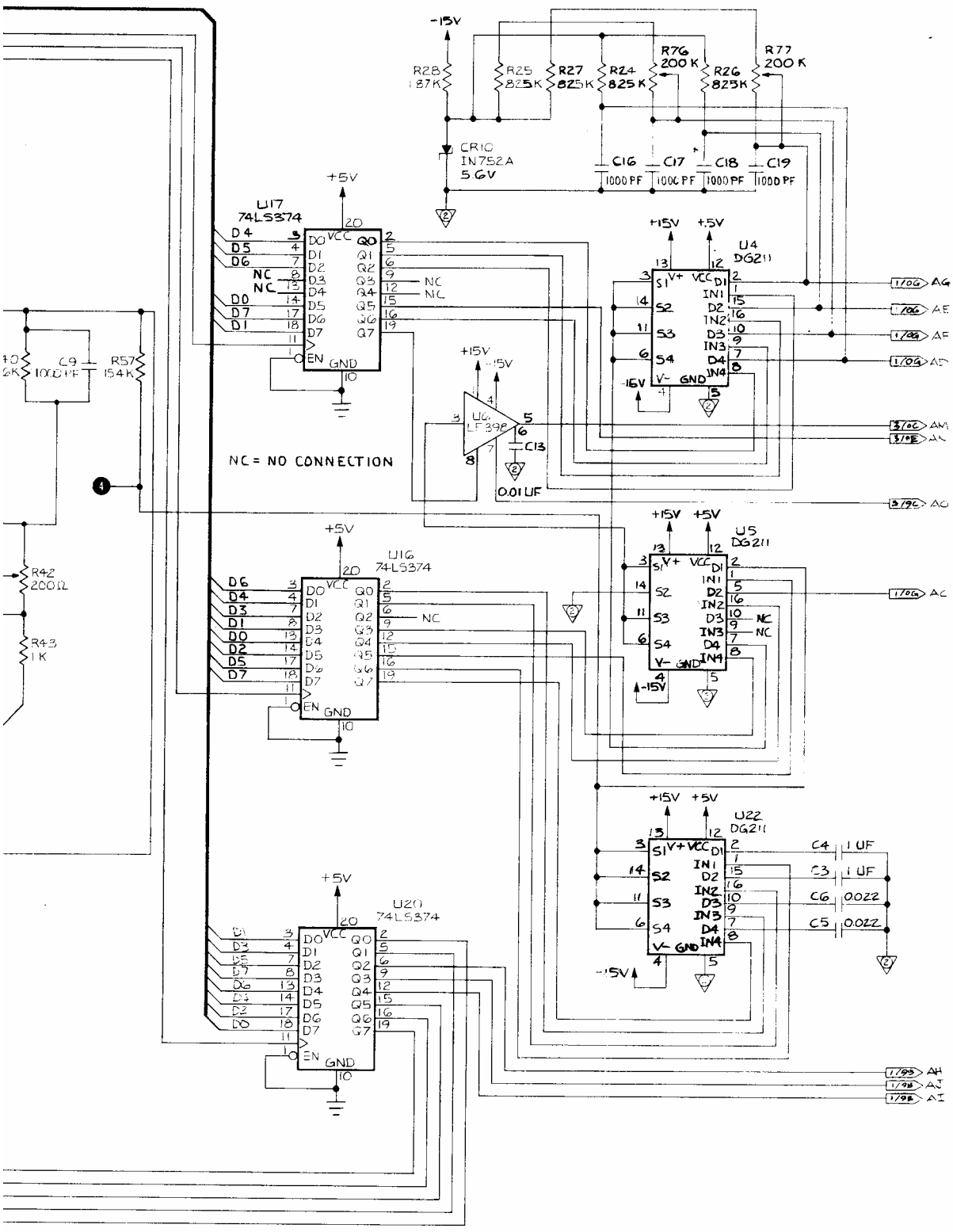
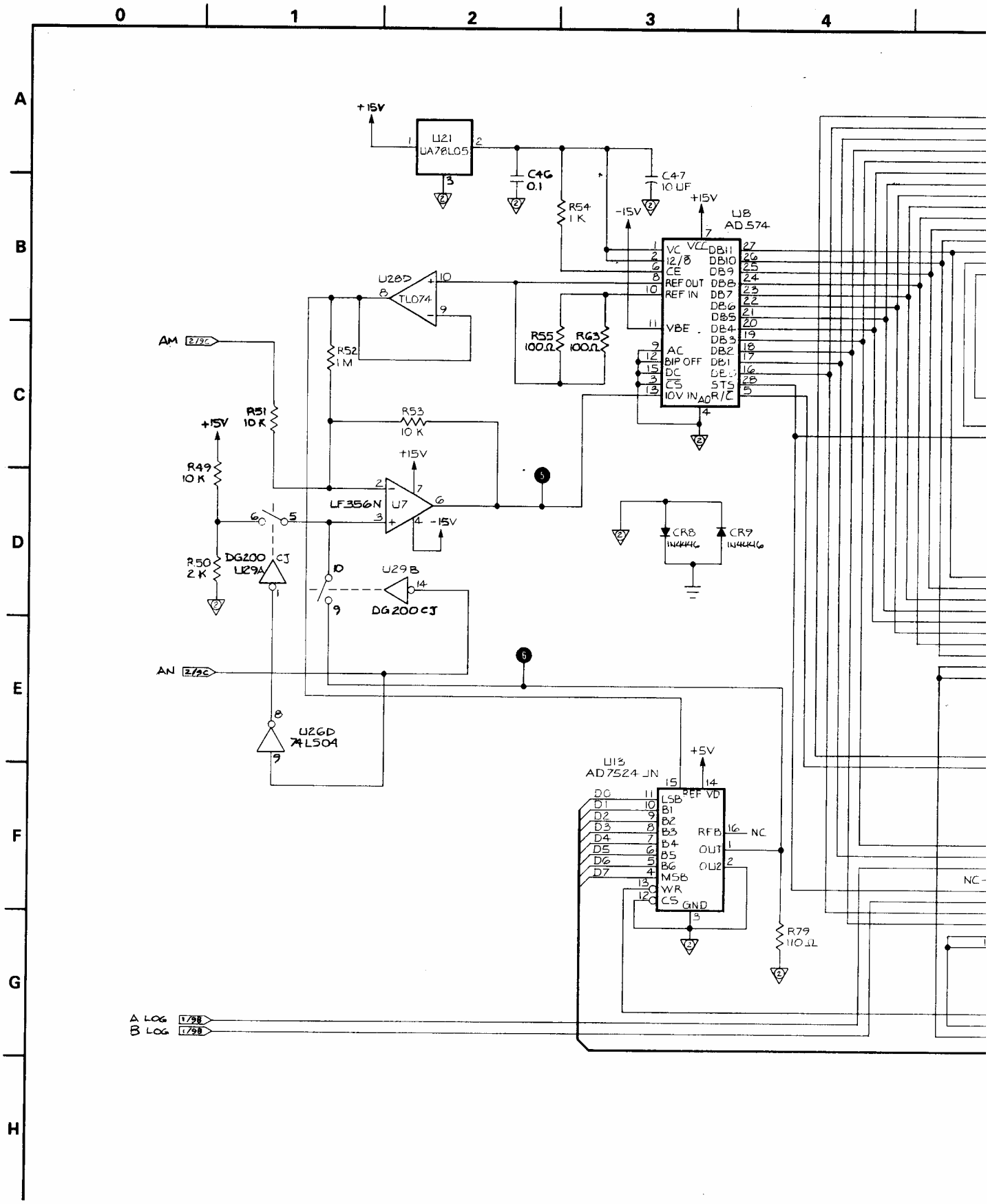


Figure 8-38. A3 Signal Channel Schematic (Continued)


+15V
U21
UA78L05
C46
0.1
C47
10 UF
R54
1 K
-15V
+15V
U8
AD574
VC
12/8
CE
REF OUT
REF IN
VBE
AC
BIP OFF
DC
CS
10V IN
VCC
A0
R/C
STS
DB11
DB10
DB9
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
U28D
TL074
R52
1 M
R55
100Ω
R63
100Ω
AM
R51
10 K
R53
10 K
+15V
R49
10 K
LF356N
U7
-15V
CR8
IN4446
CR9
IN4446
R50
2 K
DG200
U29A
CJ
U29B
DG200CJ
AN
U26D
74LS04
U13
AD7524 JN
+5V
D0
D1
D2
D3
D4
D5
D6
D7
LSB
B1
B2
B3
B4
B5
B6
MSB
WR
CS
REF VD
RFB
OUT1
OUT2
GND
NC
R79
110 Ω
A LOG
B LOG

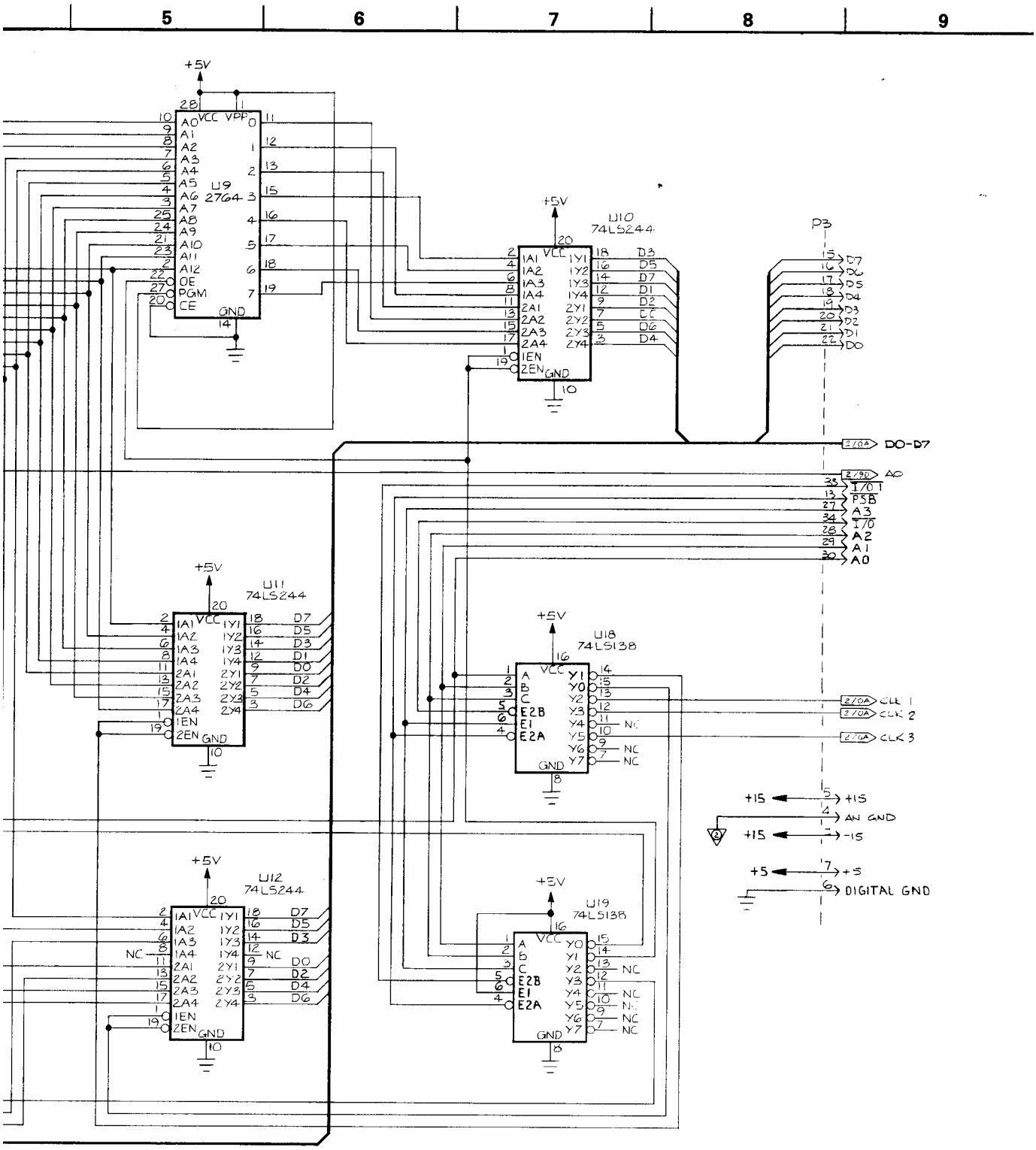


Figure 8-38. A3 Signal Channel Schematic (Continued)

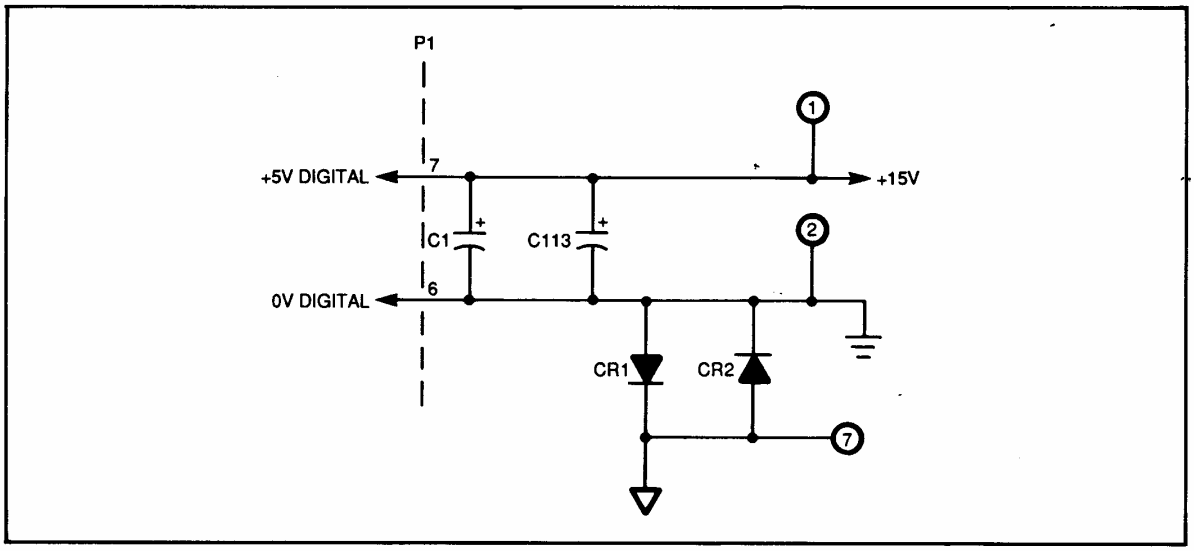


Figure 8-39. Power Supply to A4 Digital Circuitry

8-7.4 A4 Sweeper Board PCB

The A4 Sweeper PCB can be separated into three distinct sections:

1. Digital decoding, digital-to-analogue conversion, ramp generation.
2. YIG oscillator drivers, YIG bias supply, YIG tune supply, main analogue supplies and step attenuator driver.
3. ALC, plus slope and temperature compensation.

The A4 block diagram is shown in Figures 8-56 and 8-57. The parts locator diagram and schematic are shown in Figures 8-58 and 8-59. Unless directed otherwise, refer to the overall block diagram (Figures 8-56 and 8-57) for the following discussions.

a. Digital Section. The digital section provides data words, decoding logic, and the frequency controlling digital-to-analogue converters (DACs).

   This section obtains its +5V supply from the A9 Power Supply PCB through the 34-Way Insulation Displacement Connector (IDC). This general +5V supply is smoothed and decoupled by capacitors C1 and C113 (Figure 8-39). In the event of the loss of either digital ground (DGND) or analogue ground (AGND), back to back diodes CR1 and CR2 protect the circuit by providing a route from DGND to AGND.

   The first part of this section provides data words to the 10- and 12-bit DACs. Two separate 8-bit bytes of data are lumped together to form a single 12-bit data word. This is achieved by storing the 4 least-significant bits (LSBs) into a latch, then releasing the 4-bit nibble along with the most significant 8-bit byte to form the 12-bit data word. The IC number, DAC description, and port numbers for this section are shown below.

IC	DAC	Port No.
U11	Sweep	0A0H/0A1H
U14	Width	0A2H/0A3H
U17	Center	0A4H/0A5H
U18	Error	0A6H/0A7H
U39	ALC/Power	0A8H/0A9H
U38	Slope and Temperature Correction	0A8H/0A9H

The second part of this section contains the decoding logic ICs: U4, U5, U6, U7, and U8 (Figure 8-40). These decoding logic ICs provide clock signals to:

1. The 10- and 12-bit DAC latches U9, U10, U12, U13, U15, and U16.
2. U1 and U2, 8-bit latches that are used mainly to control FET switches and driver ICs. A more detailed functional description of these two latches is provided in Table 8-10.
3. U3, a 4-bit latch.

The clocks for full word applications are provided by U7. The other clocks are for byte applications.

The third part of this section contains the four frequency controlling DACs: U11 (sweep), U14 (sweep width), U17 (center), and U18 (error). U18 is a 12-bit DAC that gives greater frequency resolution. All the DACs are microprocessor controlled.

Table 8-10. U1 and U2 Description

Bit	Port	IC	PIN	Function
7	B1	U1	19	FM Coil sweep
6	B1	U1	16	No Connection
5	B1	U1	2	Unleveled LED Gate Signal
4	B1	U1	5	No Connection
3	B1	U1	15	Main Coil Sweep
2	B1	U1	12	RF Off
1	B1	U1	6	ALC Level 1
0	B1	U1	9	ALC Level 2
7	B0	U2	19	Att'n B (U30#1)
6	B0	U2	16	Att'n A (U29#1)
5	B0	U2	2	Att'n D (U32#1)
4	B0	U2	5	Att'n C (U31#1)
3	B0	U2	15	No Connection
2	B0	U2	12	No Connection
1	B0	U2	6	No Connection
0	B0	U2	9	CW Filter

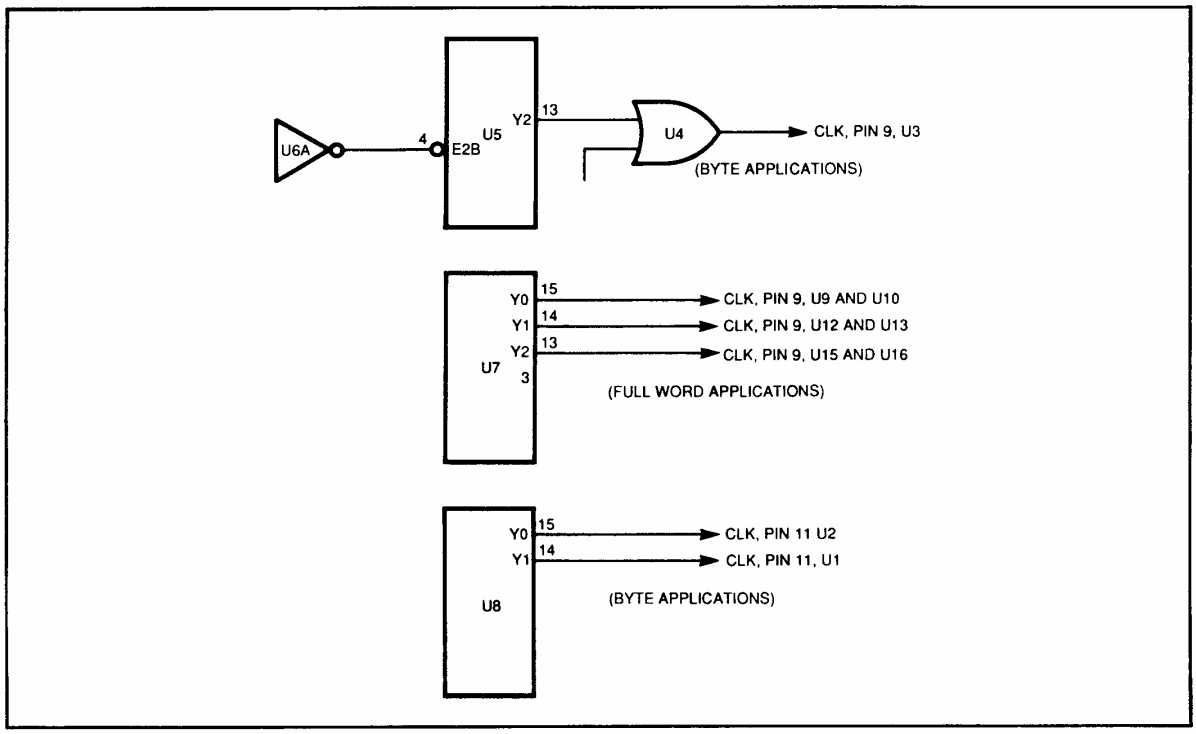


Figure 8-40. Decoding Logic ICs

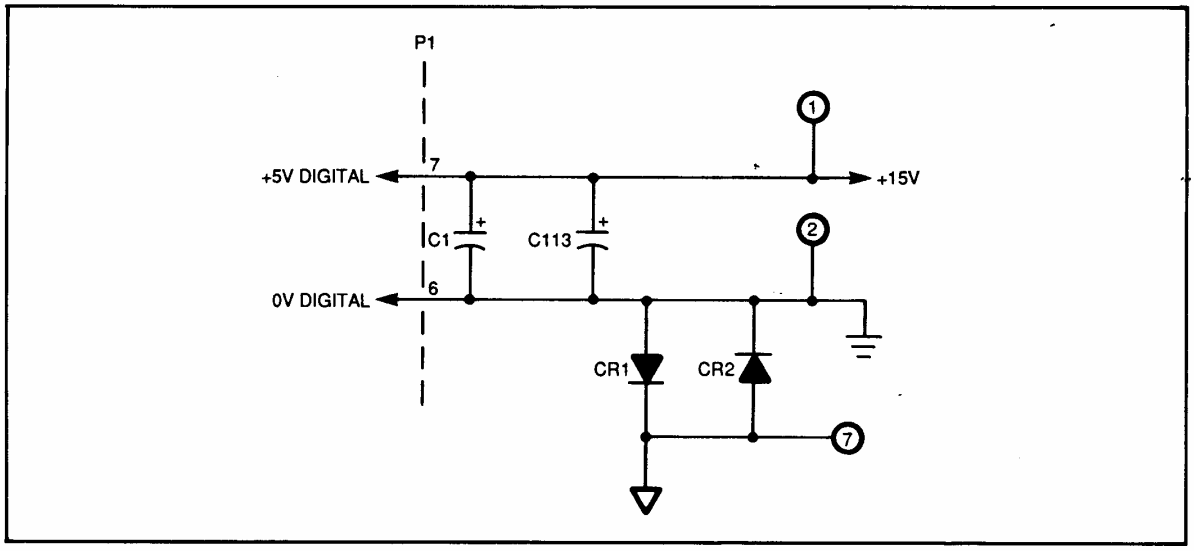


Figure 8-39. Power Supply to A4 Digital Circuitry

8-7.4 A4 Sweeper Board PCB

The A4 Sweeper PCB can be separated into three distinct sections:

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The A4 block diagram is shown in Figures 8-56 and 8-57. The parts locator diagram and schematic are shown in Figures 8-58 and 8-59. Unless directed otherwise, refer to the overall block diagram (Figures 8-56 and 8-57) for the following discussions.

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   The first part of this section provides data words to the 10- and 12-bit DACs. Two separate 8-bit bytes of data are lumped together to form a single 12-bit data word. This is achieved by storing the 4 least-significant bits (LSBs) into a latch, then releasing the 4-bit nibble along with the most significant 8-bit byte to form the 12-bit data word. The IC number, DAC description, and port numbers for this section are shown below.

IC	DAC	Port No.
U11	Sweep	0A0H/0A1H
U14	Width	0A2H/0A3H
U17	Center	0A4H/0A5H
U18	Error	0A6H/0A7H
U39	ALC/Power	0A8H/0A9H
U38	Slope and Temperature Correction	0A8H/0A9H

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2. U1 and U2, 8-bit latches that are used mainly to control FET switches and driver ICs. A more detailed functional description of these two latches is provided in Table 8-10.
3. U3, a 4-bit latch.

The clocks for full word applications are provided by U7. The other clocks are for byte applications.

The third part of this section contains the four frequency controlling DACs: U11 (sweep), U14 (sweep width), U17 (center), and U18 (error). U18 is a 12-bit DAC that gives greater frequency resolution. All the DACs are microprocessor controlled.

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5	B1	U1	2	Unleveled LED Gate Signal
4	B1	U1	5	No Connection
3	B1	U1	15	Main Coil Sweep
2	B1	U1	12	RF Off
1	B1	U1	6	ALC Level 1
0	B1	U1	9	ALC Level 2
7	B0	U2	19	Att'n B (U30#1)
6	B0	U2	16	Att'n A (U29#1)
5	B0	U2	2	Att'n D (U32#1)
4	B0	U2	5	Att'n C (U31#1)
3	B0	U2	15	No Connection
2	B0	U2	12	No Connection
1	B0	U2	6	No Connection
0	B0	U2	9	CW Filter

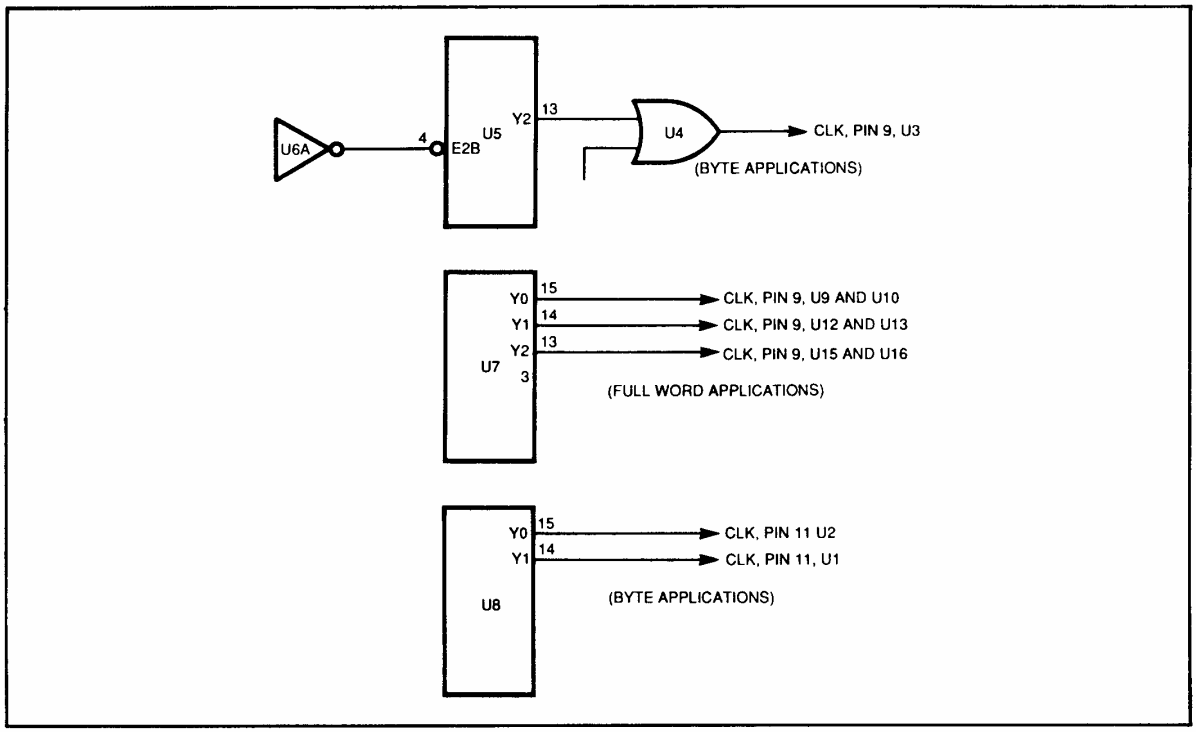


Figure 8-40. Decoding Logic ICs

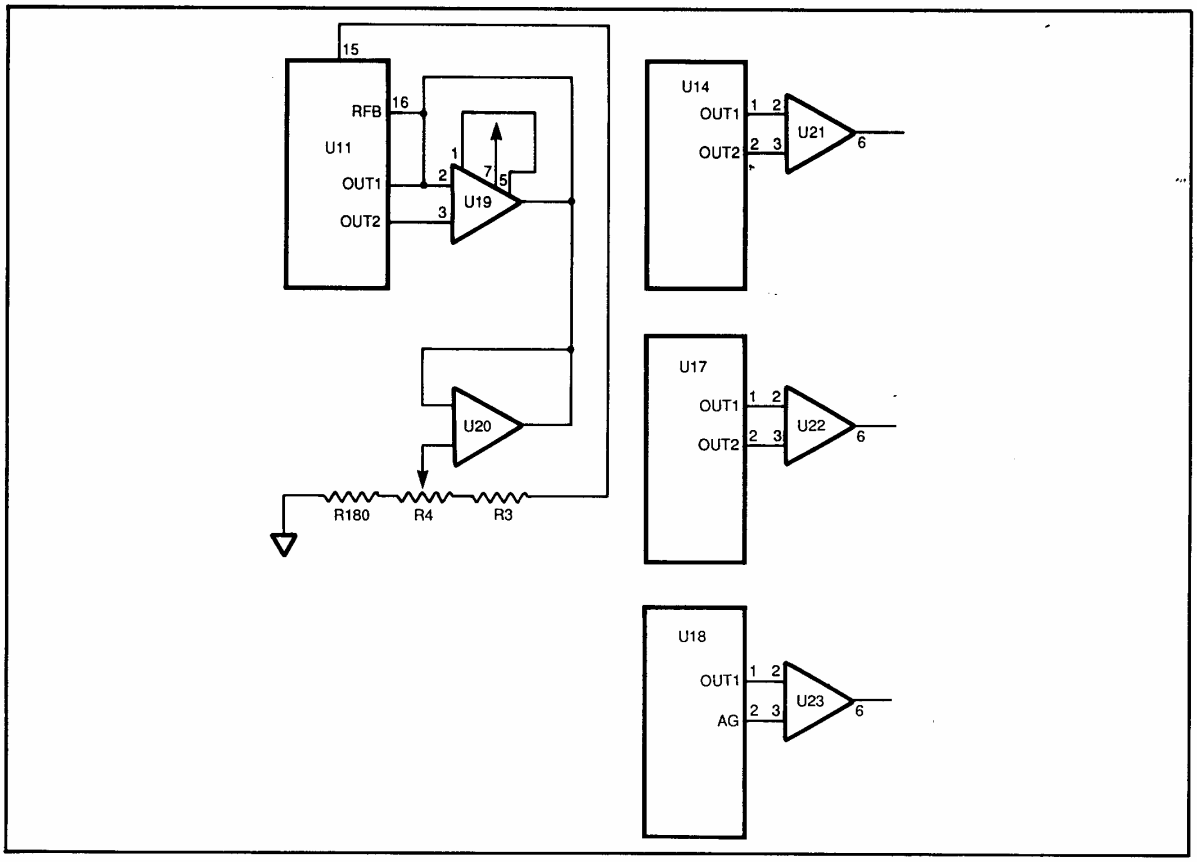


Figure 8-41. Op Amps and DACs

Op-amps U19, U21, U22, and U23 in this section are used as current-voltage converters and buffers for the DACs.

Another op-amp, U20, is used to center the sweep ramp voltage output by adjusting potentiometer R4. The primary function of U24 is to provide the + and -10V reference for the DACs and coil drivers (Figure 8-42).

b. Driver Circuits. The A4 PCB Driver Cricuitry provides the drive current and bias voltage for the YIG oscillator. The discussion of the driver circuitry is divided into six parts: (1) Main Tuning Coil Circuit; (2) FM Coil-Driver Circuit; (3) YIG Bias Circuit; (4) YIG Tuning Supply Circuit; (5) Step Attenuator/Relay Driver Circuit; and (6), Linearization Transformer.

1. The Main Tuning Coil Driver circuit operates as a voltage-to-current converter. Three signals--Main Coil Sweep, Band Start, and Center--are summed at the inverting input of U27 (Figure 8-43). The U27 output controls the current to the YIG main coil via transistor Q4.

   The current through the coil develops a proportional voltage across a sensing resistor, R49. Resistors R49 and R50 form part

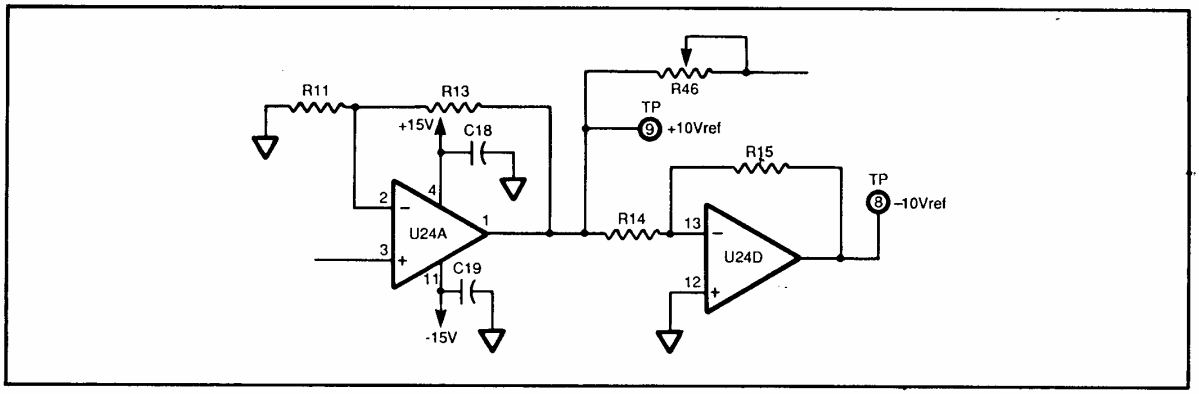


Figure 8-42. +/-10V Referency Circuitry

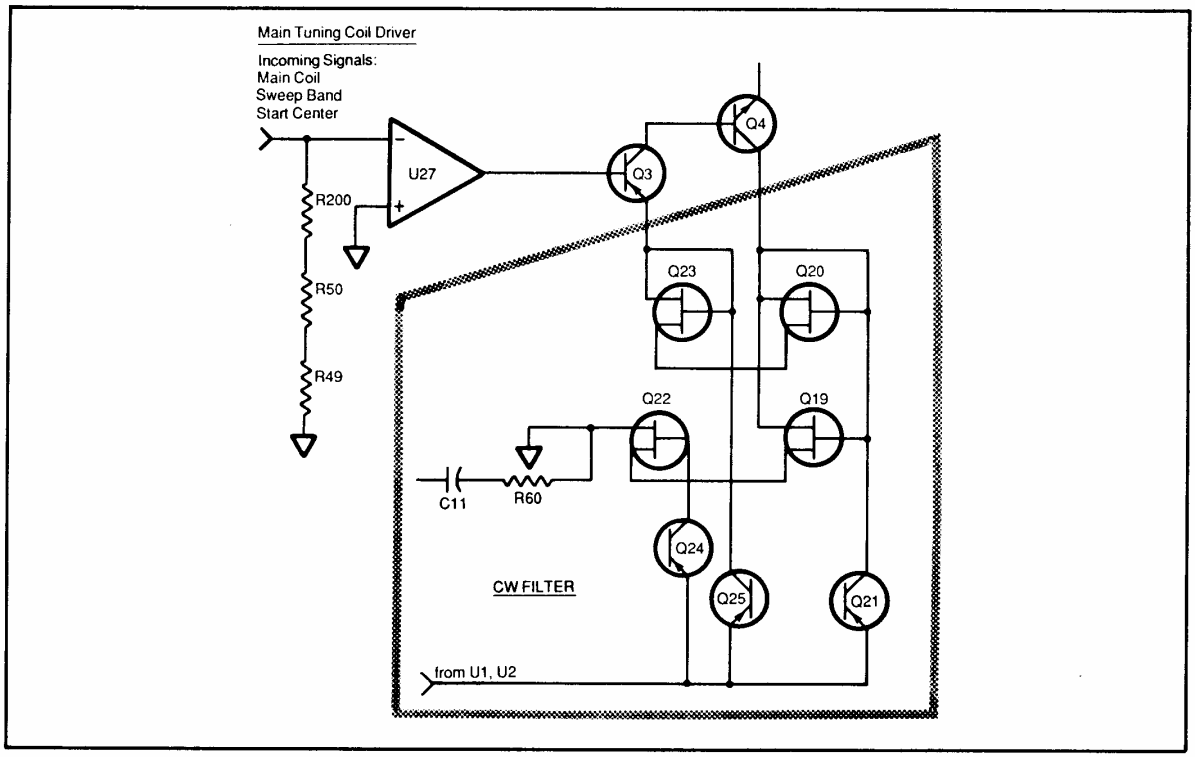


Figure 8-43. Main Tuning Coil Driver and CW Filter Circuitry

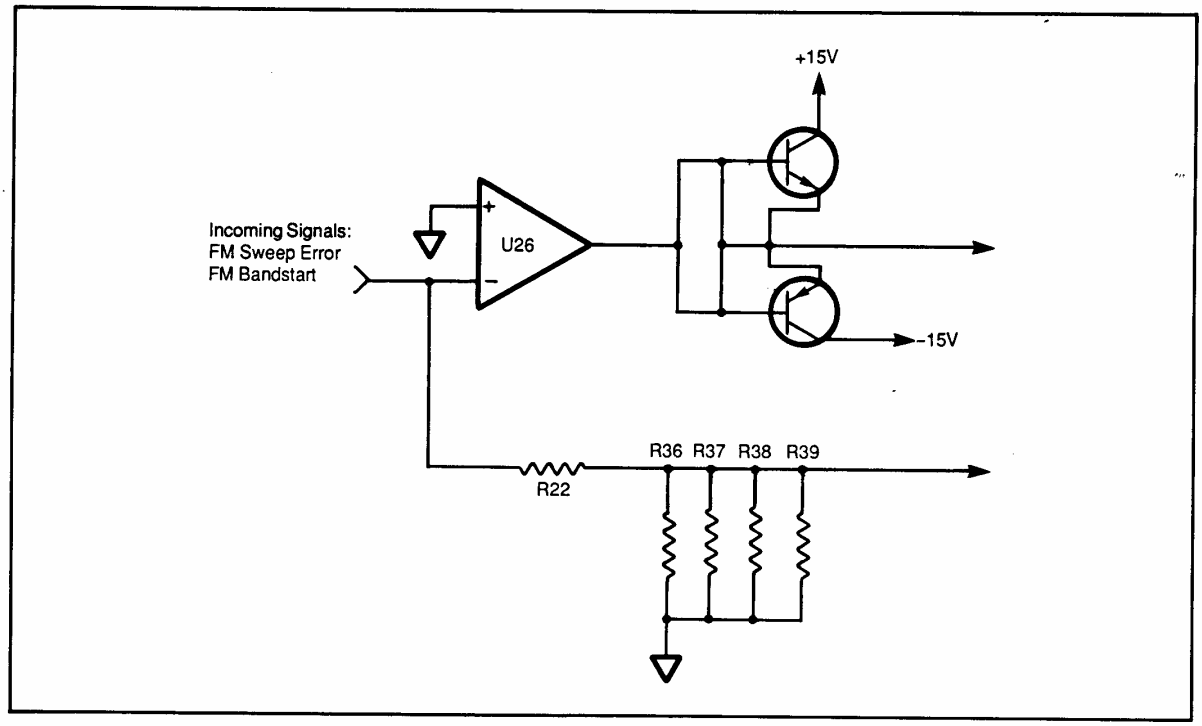


Figure 8-44. FM Coil Driver Circuitry

of the feedback loop, with R50 functioning as the gain-determining resistor and R200 as the select-on-test resistor for the YIG.

The CW filter is also included in the main coil driver circuitry. When the CW filter is activated (when the sweep width is less than 40 MHz), the FET switch arrangement of Q19 to Q25 closes. The C41-R60 filter network then bandwidth-limits the YIG tuning-coil, current-driver loop by introducing an additional negative-feedback path. This path filters the noise current flowing through the coil and quiets the YIG oscillator frequency output.

2. The FM Coil-Driver circuit is also a voltage to current converter. Signals FM Sweep, Error, and FM Band-Start are summed at the inverting input of voltage amplifier U26 (Figure 8-44). The output of the amplifier drives the current amplifier circuit of Q1 and Q2.

The output of the Q1-Q2 circuit supplies current to the YIG oscillator FM coil. The FM coil current returns to ground via the current sensing resistors R36, R37, R38, and R39. The voltage drop across these parallel resistors is proportional to the current through the FM coil. The feedback gain-determining resistor is R22.

Both the Main and FM coil-drivers (U26 and U27) have low pass T-filter networks incorporated into their input circuits to reduce the level of noise, hence the level of residual FM.

Power for the analog circuitry comes through connector P6. This includes regulated +18V and -18V supplies, the YIG Tune Supply voltage (0V, -18V), and the +25V required by the step attenuator relays and the YIG heater. The analog +15V and -15V supplies provide 1.5 amps and are re-regulated on the Sweeper Board from the +/-18V rails by voltage regulators U33 and U34 (Figure 8-45).

Diodes CR53 and CR54, which are placed between the input and the output of the regulators, act as protection for the regulators in the event of power down reverse biasing. Another regulator, U35 (Figure 8-46), supplies power to the 1 MHz to 1 GHz Down Converter. The output of U35 is +9V. For the 10 MHz to 2 GHz down converter, a +15V supply is required.

3. The YIG Bias circuit (Figure 8-47) provides the -5V required by the YIG oscillator. Resistors R68 and R70 act as a voltage divider, setting up the bias voltage at the inverting input of U28. The output of U28 drives Q10 and Q11, resulting in the desired -5V output. Current overload shutdown is provided by transistors Q8 and Q9.

4. The YIG Tune Supply Circuit supplies the Main Coil Driver Circuity with the -15V needed to tune the YIG oscillator. It takes a separate -18V supply voltage and, using a simple series regulator circuit based around Q14 (Figure 8-48), gives a regulated -15V output. The output current has been limited to a value of approximately 1.6A at -15V. The current limiting resistor is R88.

5. The Step Attenuator/Relay Driver circuitry (Figure 8-49) consists of four 8-pin ICs: U29, U30, U31 and U32. These ICs are dual, positive-AND circuit, Power Drivers. Each power driver is capable of driving one relay. Diodes CR15 through CR30 protect the ICs against back EMF from the relay coils.

   When a logic 0 is present at the input (pin 1) of U29 thru U32, the relays will be energized. Conversely, when a logic 1 is present, the devices are de-energized.

6. The Linearization Transformer is actually mounted on the RF Deck. It is included here because it balances out the mutual inductance of the main YIG tuning coil and the FM coil in the YIG.

   One winding of a transformer is placed in series with the main coil winding, and the other winding of the transformer is placed in series with the FM coil winding in antiphase, hence balancing out any induced EMF.

c. Automatic Level Control (ALC).

The third section of the A4 Sweeper Board consists of the ALC circuitry. This, along with RF components mounted on the RF Deck, provides for the automatic leveling of the RF output power.

The RF output from the YIG oscillator is applied to the RF coupler/detector (in the down converter block) via the PIN Modulator mounted inside the down converter. A sample of the RF power signal (which is attenuated by approximately 16 dB) is coupled to the RF detector.

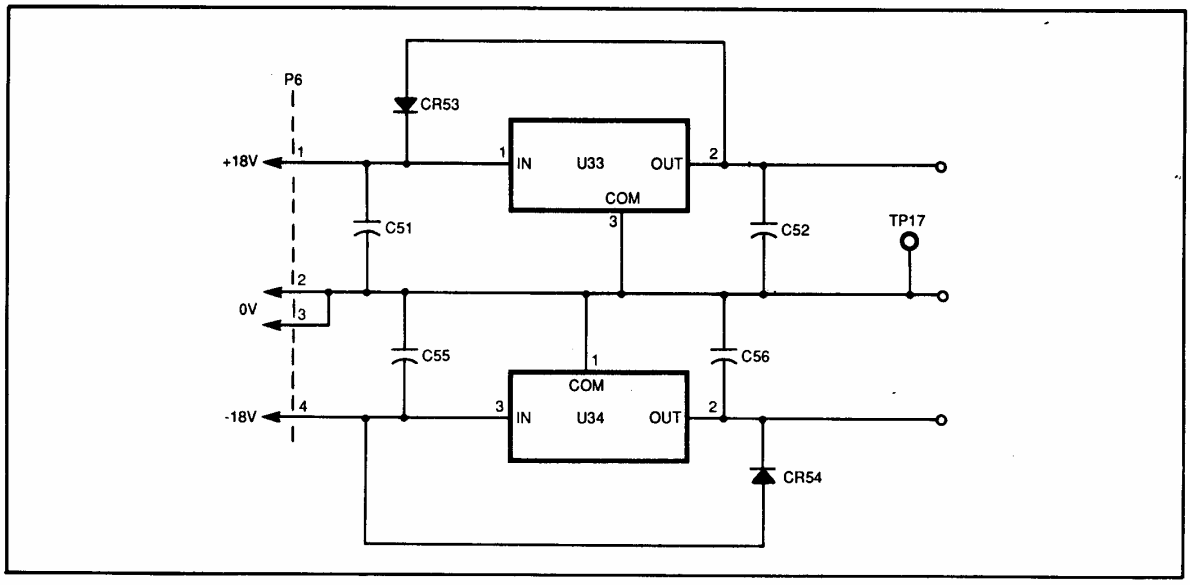


Figure 8-45. Analog Circuitry Power; +/-18V Rails

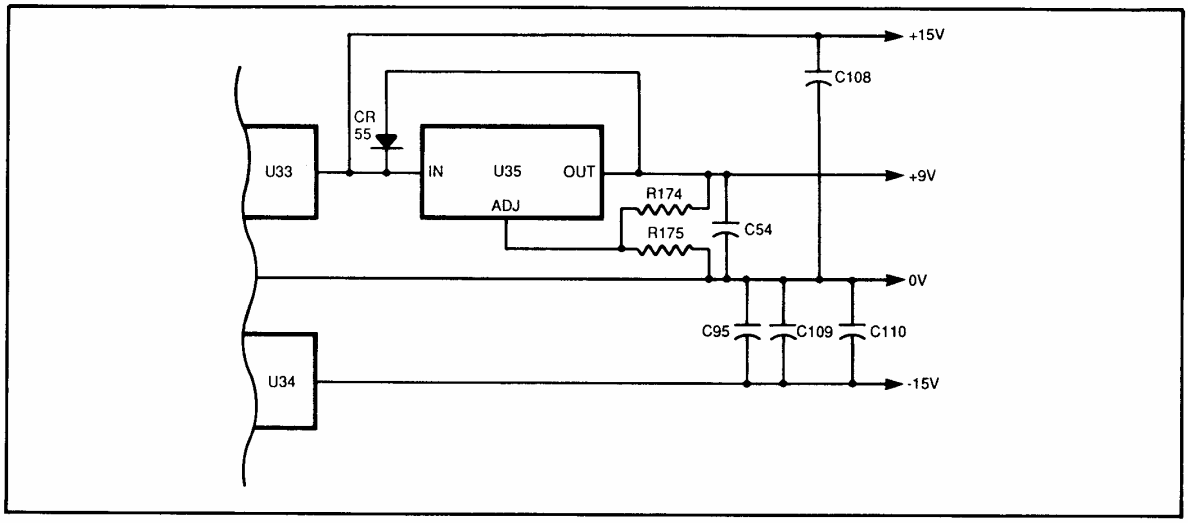


Figure 8-46. Power to Down Converter

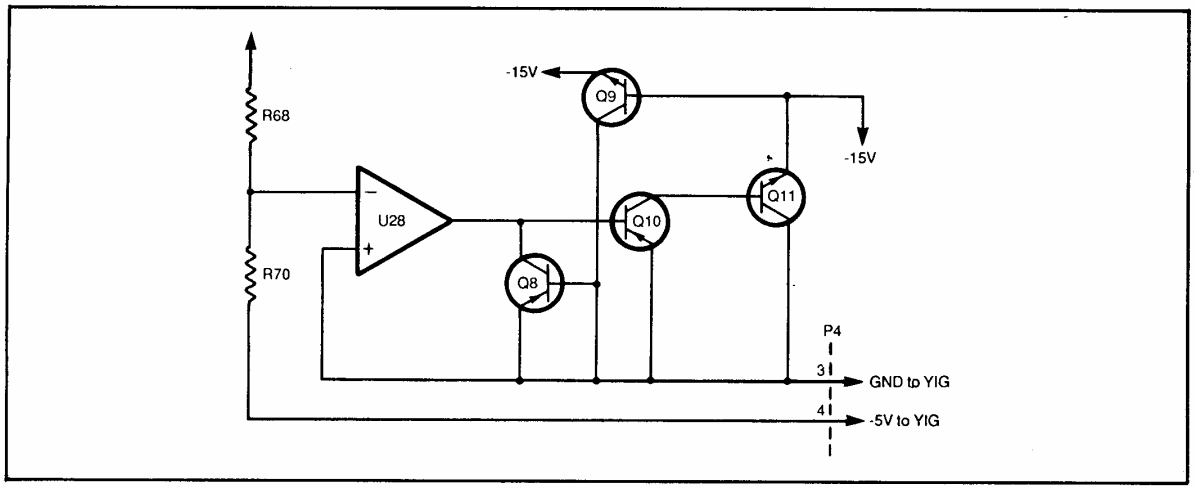


Figure 8-47. YIG Bias Circuit

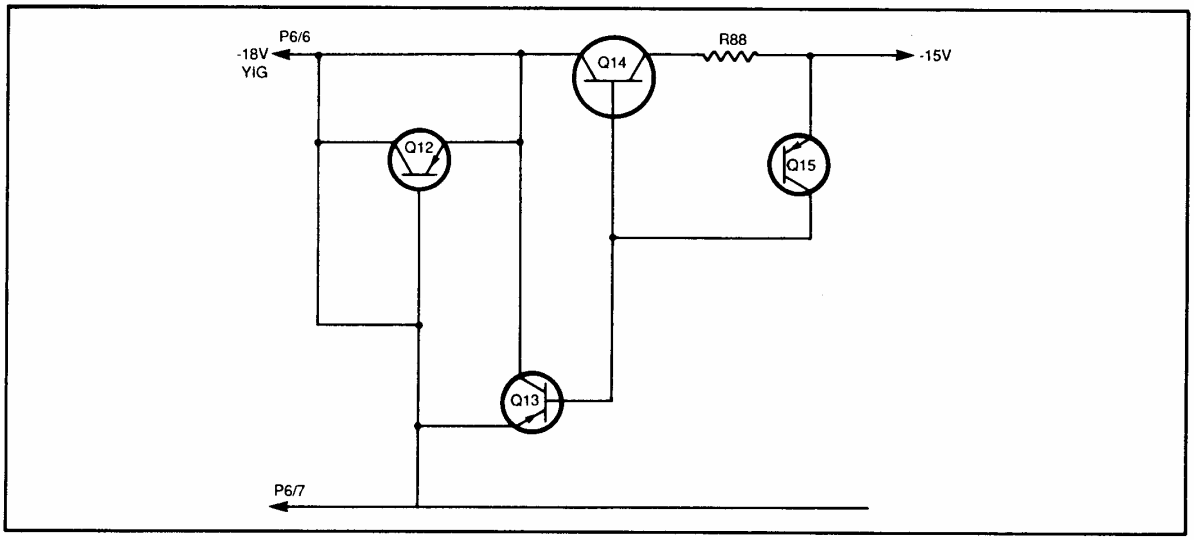


Figure 8-48. YIG Supply Circuit

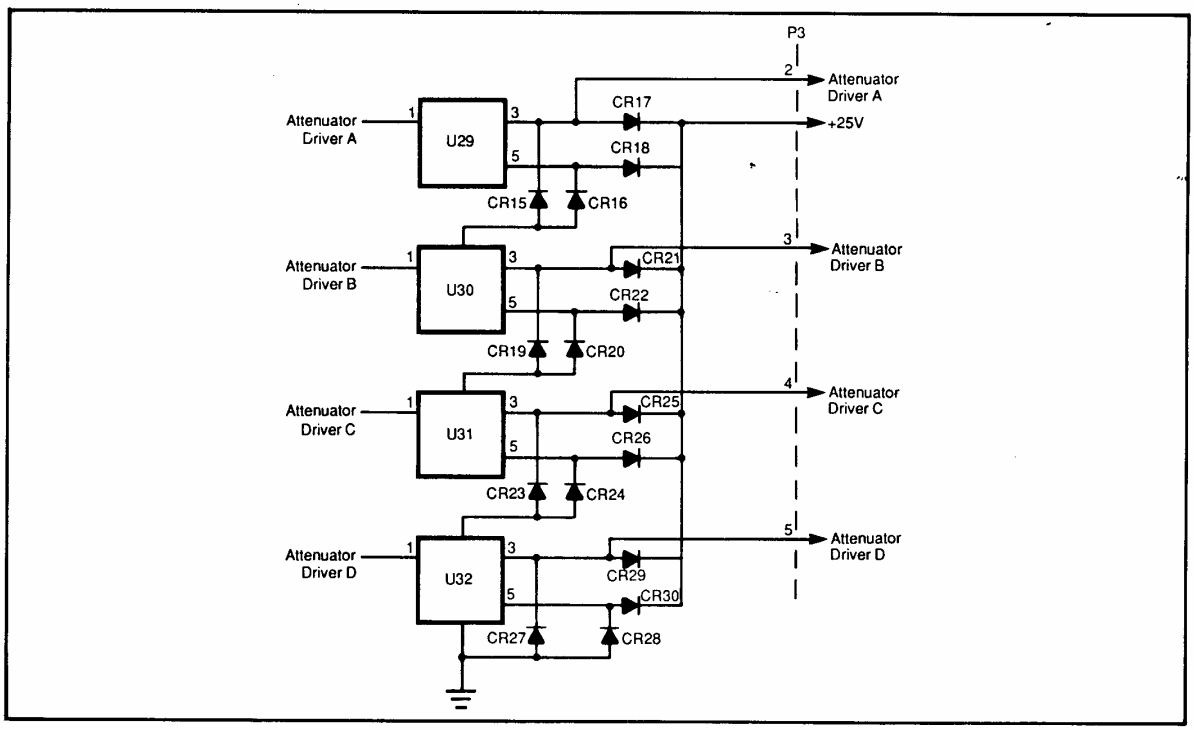


Figure 8-49. Step Attenuator/Relay Driver Circuit

The detector output signal is amplified by U46 and U47 (Figure 8-50). The signal is then fed into a summing junction (R110, R109, and R113) where it is summed with the ALC Power, Slope, and Temperature Compensation voltages.

The output of the ALC DAC, U39, is the analog voltage representation of the power which has been selected from the front panel. A stable 6.2V is provided to the ALC DAC V_{ref} from the output of U41D, the voltage reference circuit.

When a power level is selected from the control panel, the processor sends a 10-bit word to U39. The same word also goes to the ALC Slope and Temperature Compensation DAC, U38. This way, the correct proportion of the signal is summed at the inverting input of the augmenting amplifier, (Level Amp, U42).

The output of the U42 Level Amp then passes into the Shaper/Driver Amp, U43 and the unleveled LED drive circuitry (Figure 8-51). The U43 Shaper/Driver circuitry is designed to linearize, or shape, the signal, then convert it into a current for the PIN Modulator.

Normally, Q28 is switched ON and negative current flows to the pin switch to control the attenuation that keeps the RF output flat. During retrace, when the RF is switched OFF (for Signal Channel autozeroing), Q28 is switched OFF. Meanwhile, Q29 is turned ON, allowing a positive bias-current to flow to the pin switch. This bias-current blocks the RF out from the YIG oscillator by approximately 80 dB.

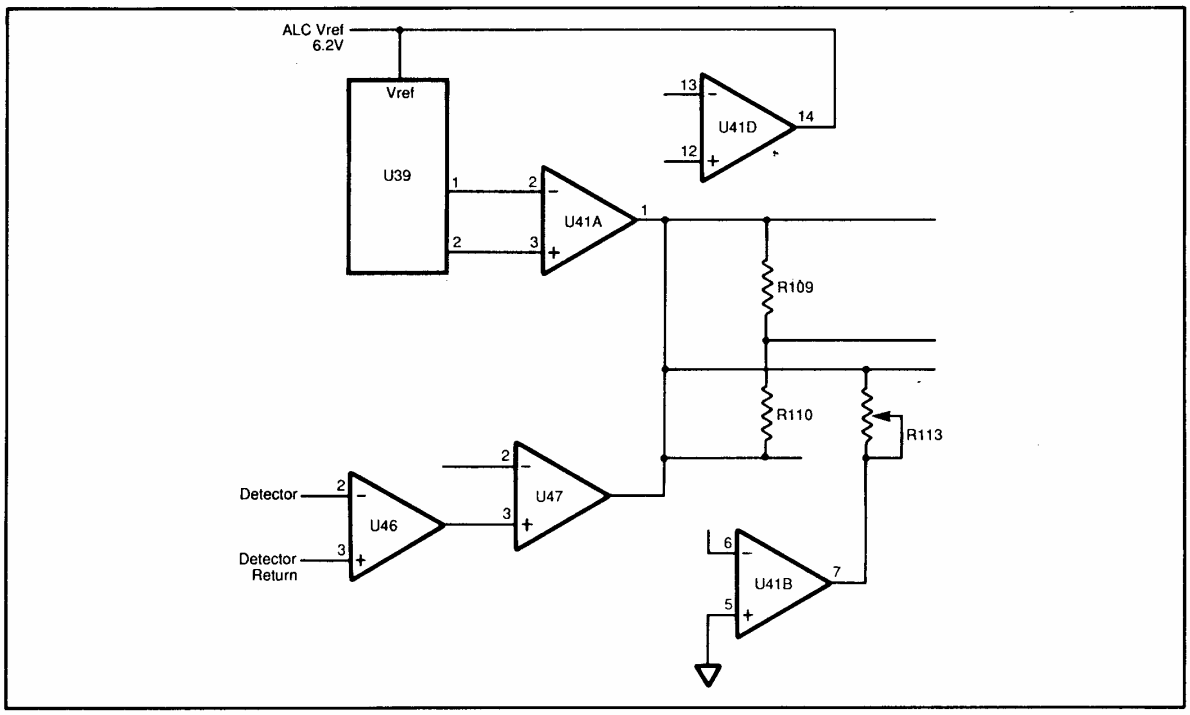


Figure 8-50. Detector Signal and Summing Junction Circuit

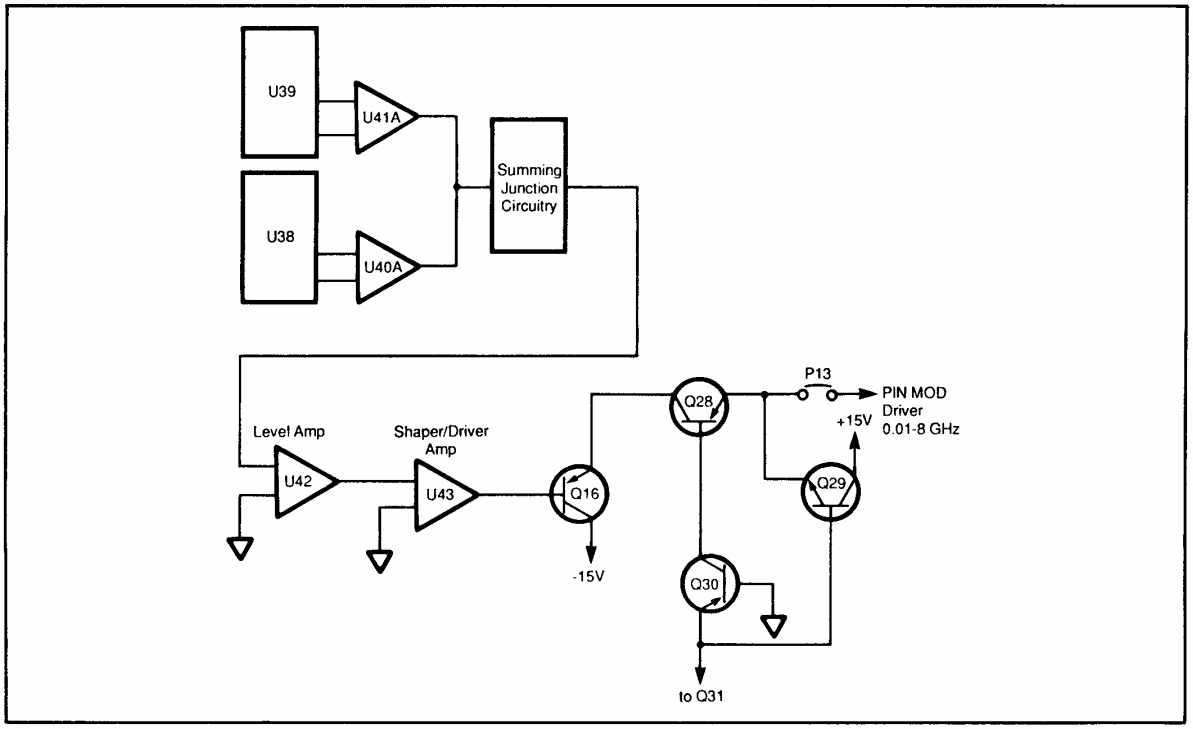


Figure 8-51. Level Amp and Shaper/Driver Amp Circuit

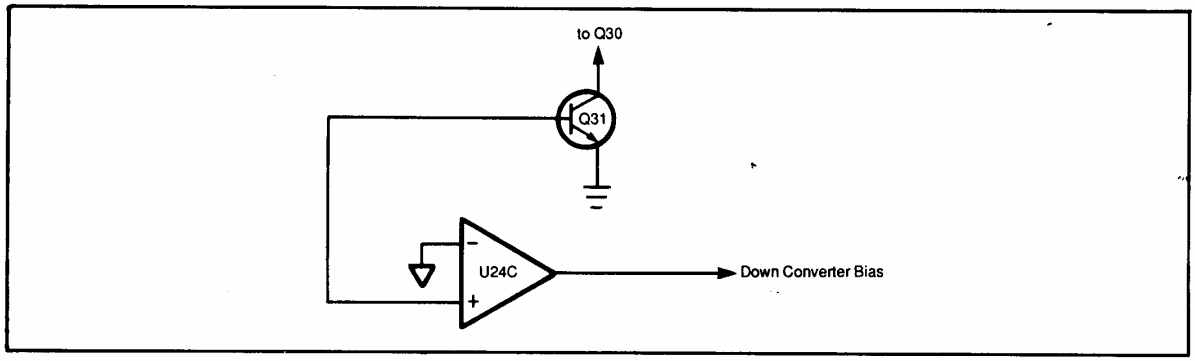


Figure 8-52. Down Converter Biasing

When the RF is ON, U24 (Figure 8-52) supplies approximately 7.5 mA of positive bias-current to the T1 port of the down converter. The down converter is mounted on the RF deck. When the RF is OFF, the output polarity of U24 is reversed, and 7.5 mA of negative bias-current is supplied to T1 of the down converter.

When the RF signal is unleveled, the UNLEVELED LED on the front panel will light if the output of U42 goes positive. When the output of U42 is positive, it means that the loop is requesting more power and is therefore unleveled. When the output of U42 is negative, the UNLEVELED LED goes OFF, which means that the loop is requesting more attenuation and is in a leveled state.

A special Retrace Pulse is injected into the UNLEVELED LED gating logic, U44 (Figure 8-53), to prevent the LED from flashing during retrace. The LED must always be OFF during Leveled periods.

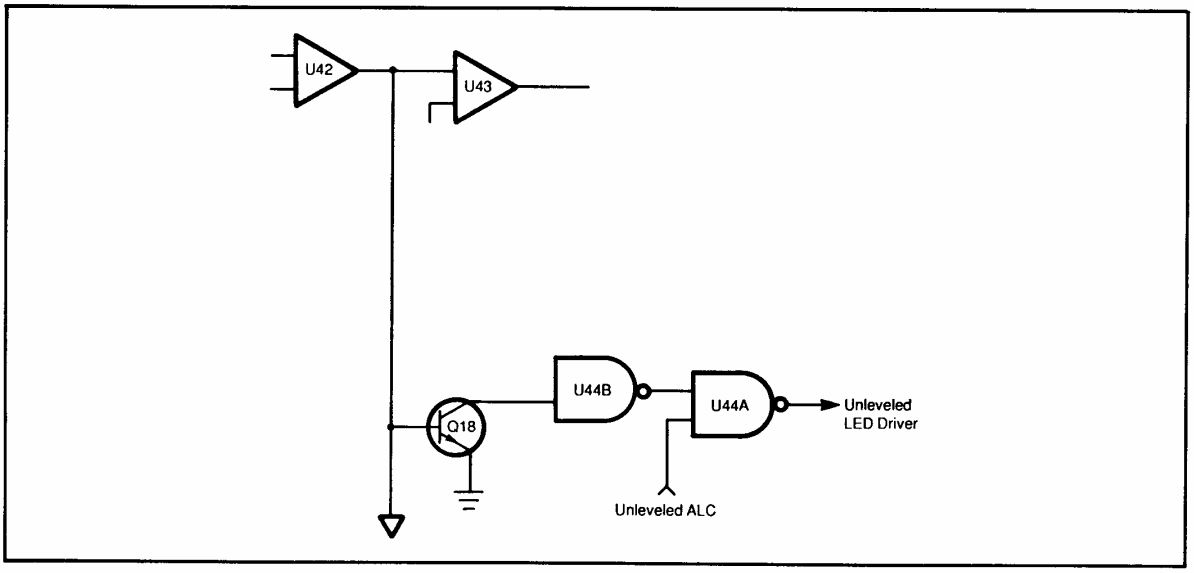


Figure 8-53. U44 Logic Gate

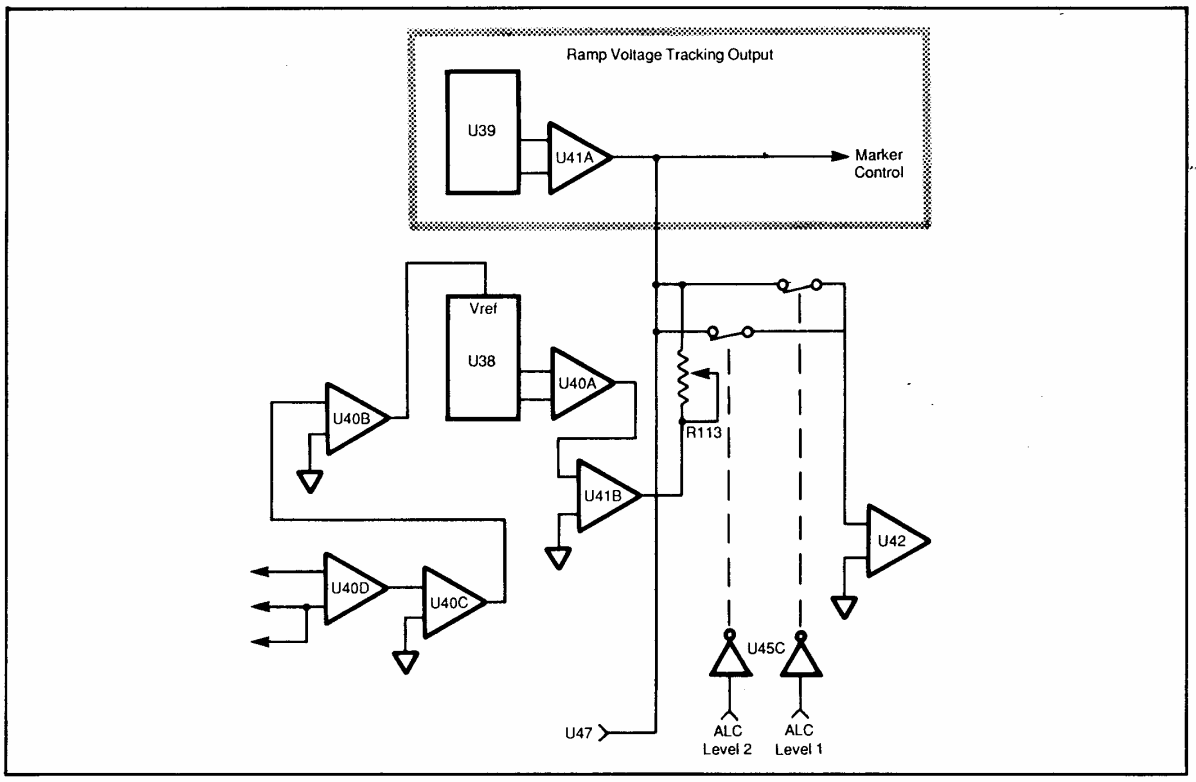


Figure 8-54. Temperature Correction and Slope Adjust Circuit/Ramp Voltage Tracking Output

The Temperature Correction and Slope Adjust Circuitry (Figure 8-54) is made up of the U40 quad op amp. Temperature correction is achieved by producing a small voltage that varies linearly with variations in temperature. This voltage is further amplified and split into hot and cold separators by the temperature compensation circuitry.

This correction voltage is then summed with the slope control voltage and fed into the Slope and Temperature Correction DAC, U38. The magnitude of the output of U38 is dependent upon the power level requirement of the instrument. Finally the signal is fed through R113 to the summing point at the Level Amp, U42. The slope is adjusted by trimming potentiometer R113.

Two sections of quad FET switch U45 are used to switch between a 0 to +10 dBm power range of the ALC and a greater than +10 dBm range. Each range requires its own slope and ALC control voltages.

The final section of circuitry is the Ramp Voltage Tracking output(Figure 8-54), U41, pin 1. This circuit provides a ramp output to the Marker Pack (A5) to maintain marker width as the power level is varied.

The output of the marker pack is fed to the sweeper board through P7. It is then latched and buffered for output to the bus by U52 and U53 (Figure 8-55).

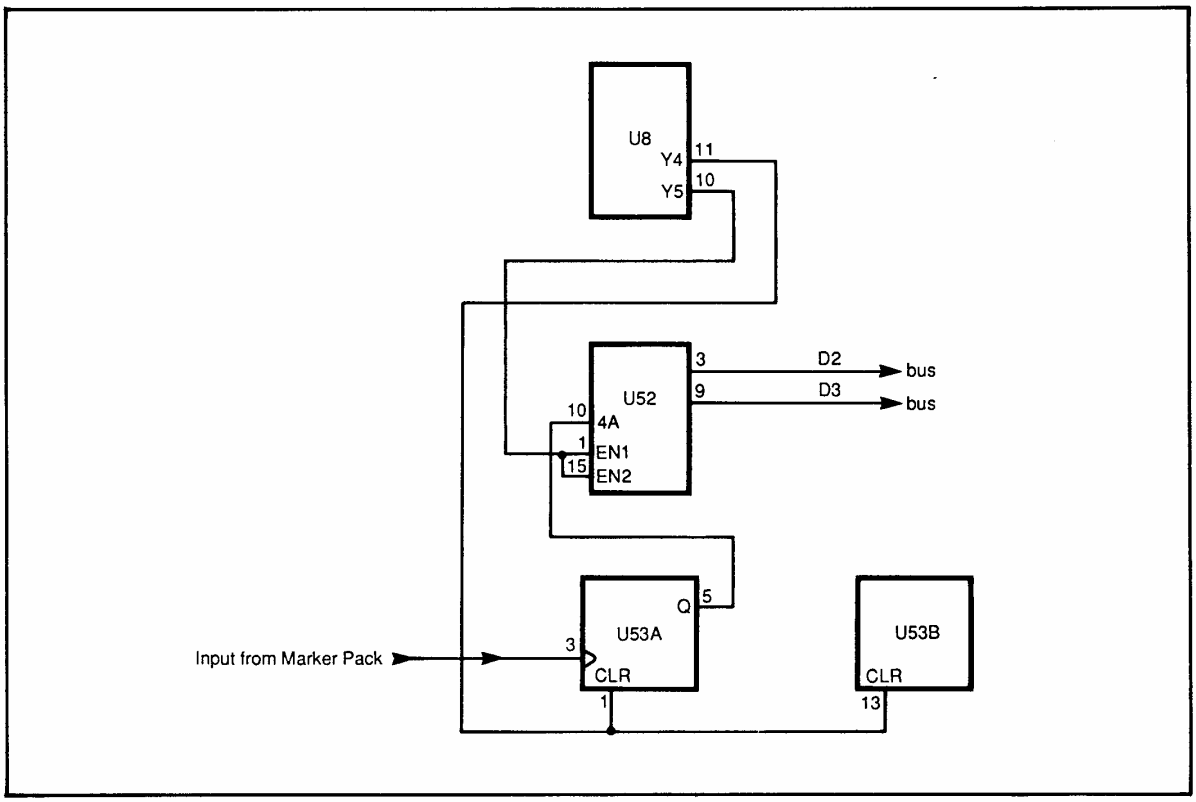


Figure 8-55. Marker Output to A4

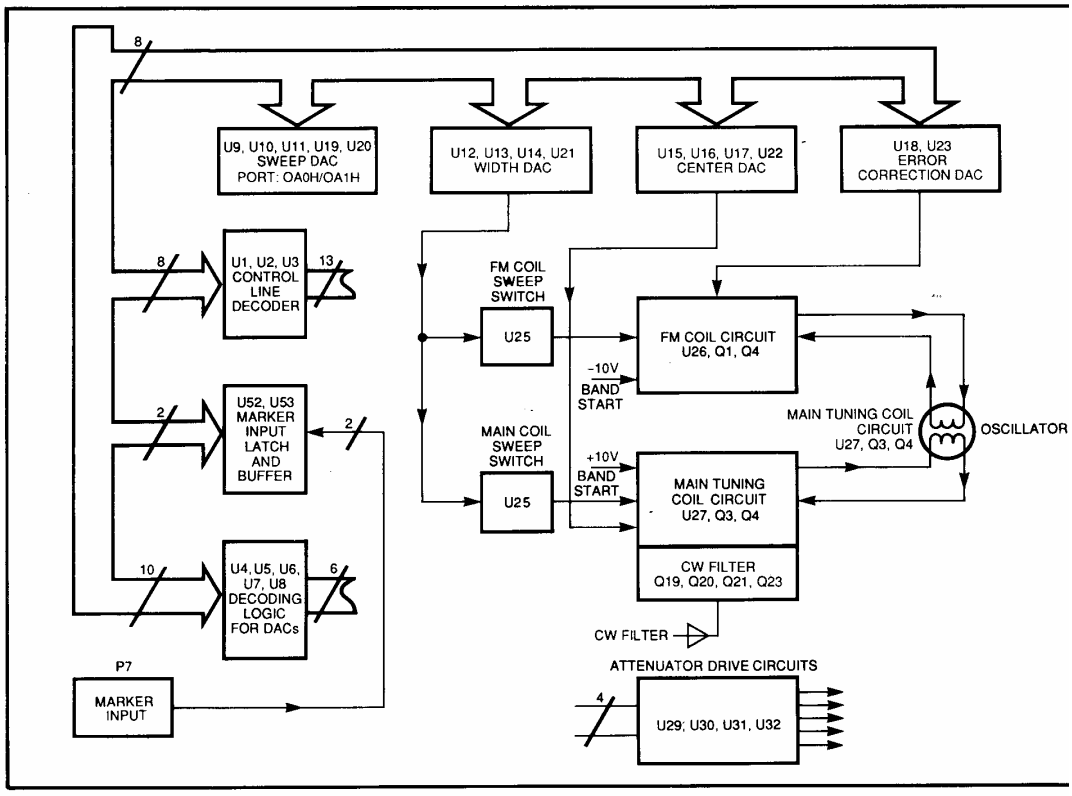


Figure 8-56. A4 Sweeper Block Diagram: Drivers, and Bias

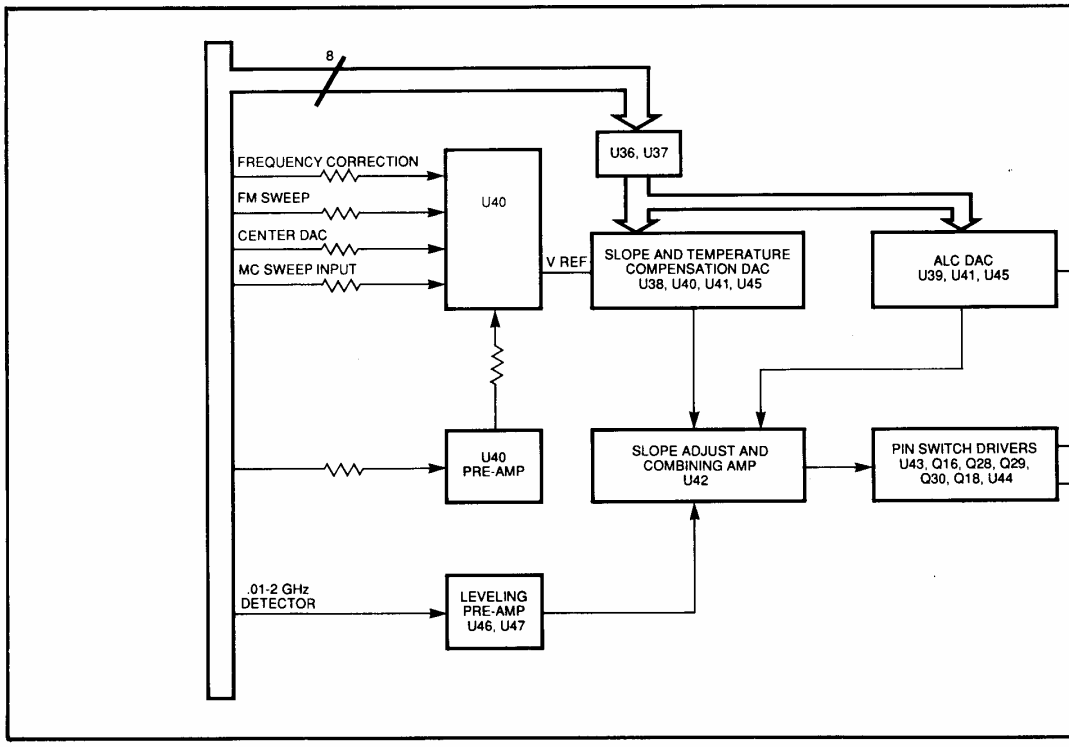


Figure 8-57. A4 Swee

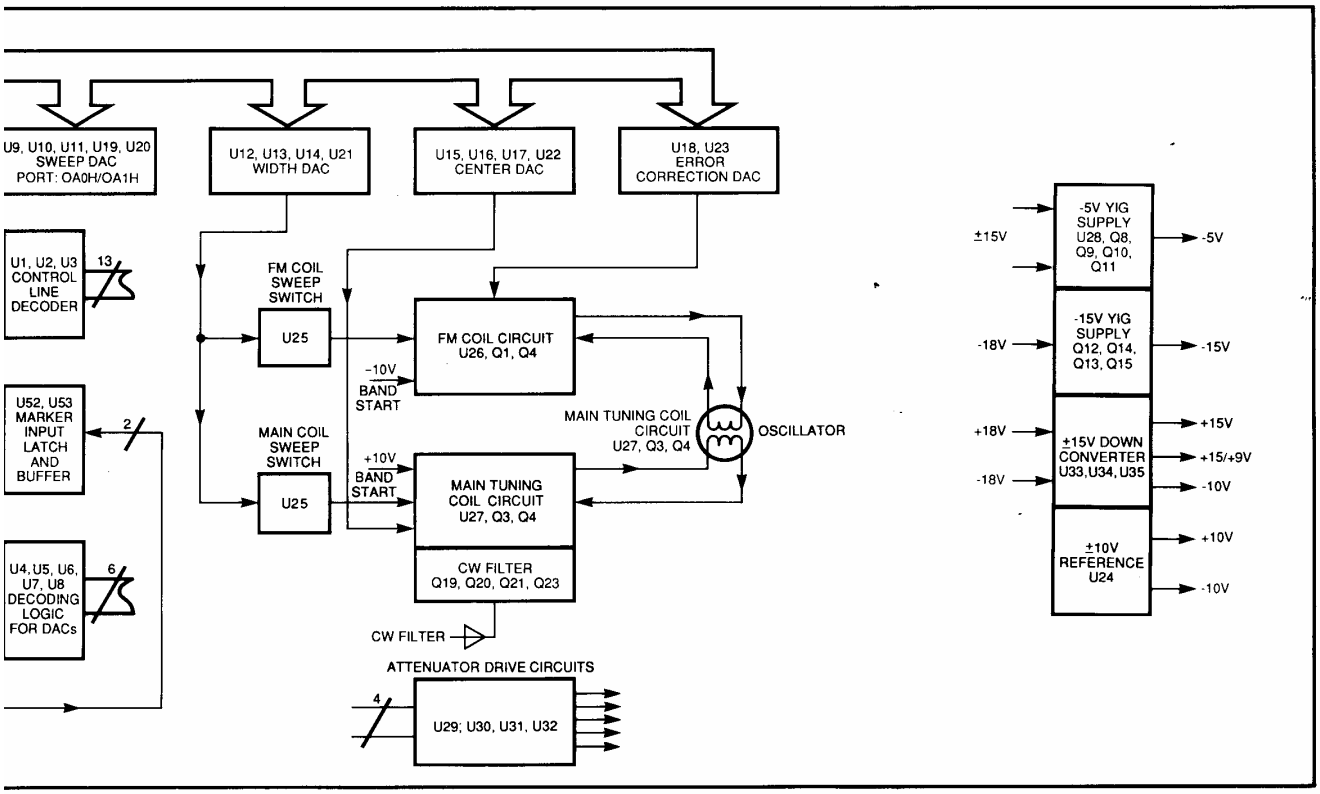


Figure 8-56. A4 Sweeper Block Diagram: Digital Circuitry, Decoding, YIG Drivers, and Bias

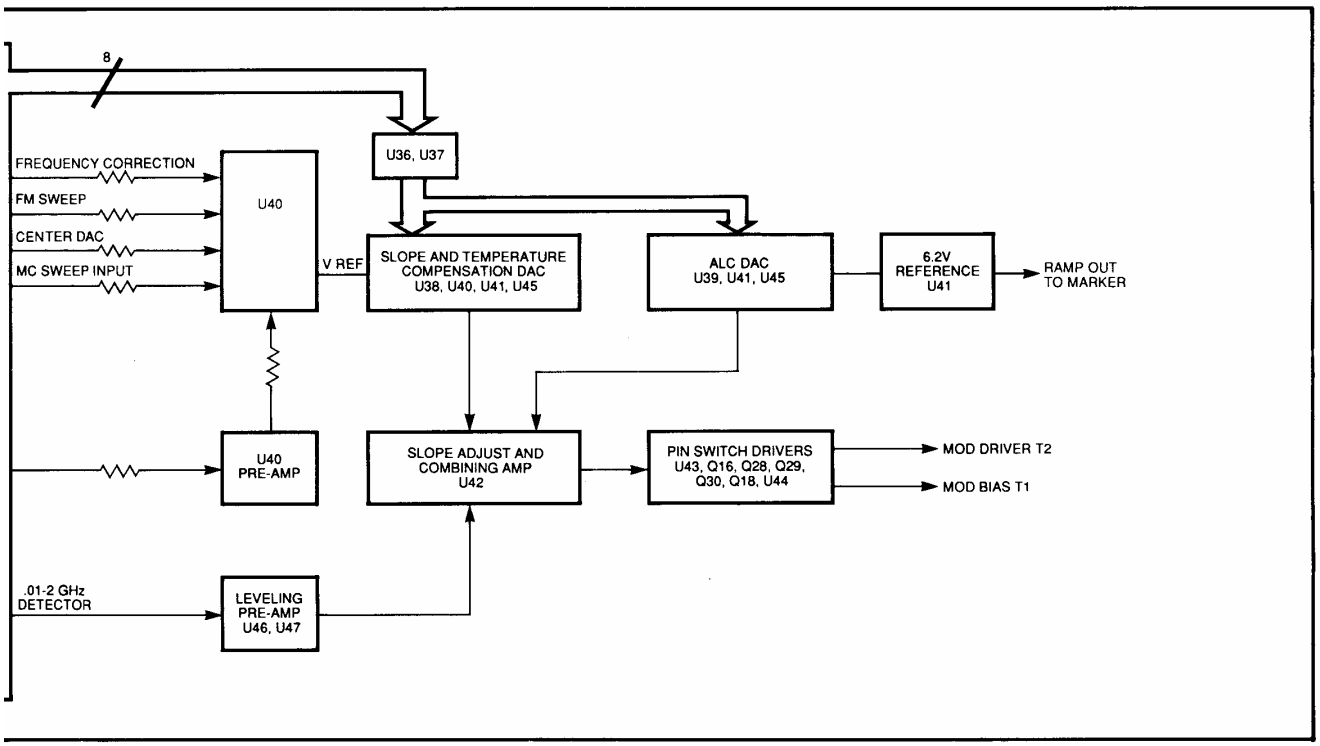
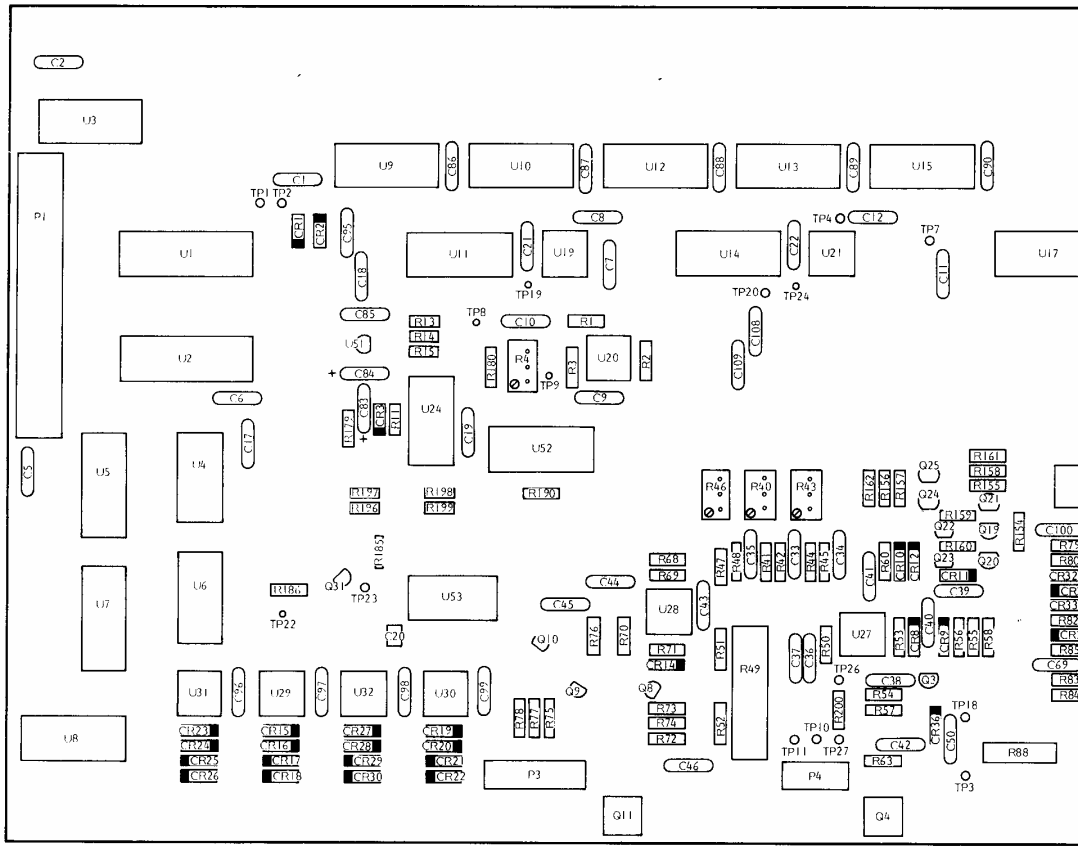


Figure 8-57. A4 Sweeper Block Diagram: ALC Circuitry


C2
U3
P1
U9
U10
U12
U13
U15
C1
TP1
TP2
U1
U11
U19
U14
U21
U17
TP19
TP20
TP24
TP4
TP7
C85
TP8
C10
R1
U2
U5
C84
U20
TP9
C9
C6
U24
U52
C5
U4
U5
C17
C19
R187
R196
R198
R199
R190
R46
R40
R43
Q25
Q24
Q21
Q22
Q23
Q20
U6
U7
Q31
TP23
TP22
U53
C44
C45
U28
C43
R68
R69
R71
R74
R72
R76
R70
R47
R48
C35
R41
R42
C33
R44
R45
C34
C41
R60
R61
C39
C40
R53
R54
R57
C38
Q3
TP26
U27
R49
R51
R52
C37
C36
R50
R200
TP10
TP11
TP27
C42
R63
C46
TP18
C36
C50
TP3
R88
U31
U29
U32
U30
C96
C97
C98
C99
Q6
Q8
Q9
R75
R77
R73
CR23
CR24
CR25
CR26
CR15
CR16
CR17
CR18
CR27
CR28
CR29
CR30
CR19
CR20
CR21
CR22
U8
P3
P4
Q11
Q4
C100
R75
R80
CR32
CR33
R82
R83
C69
R81
R84

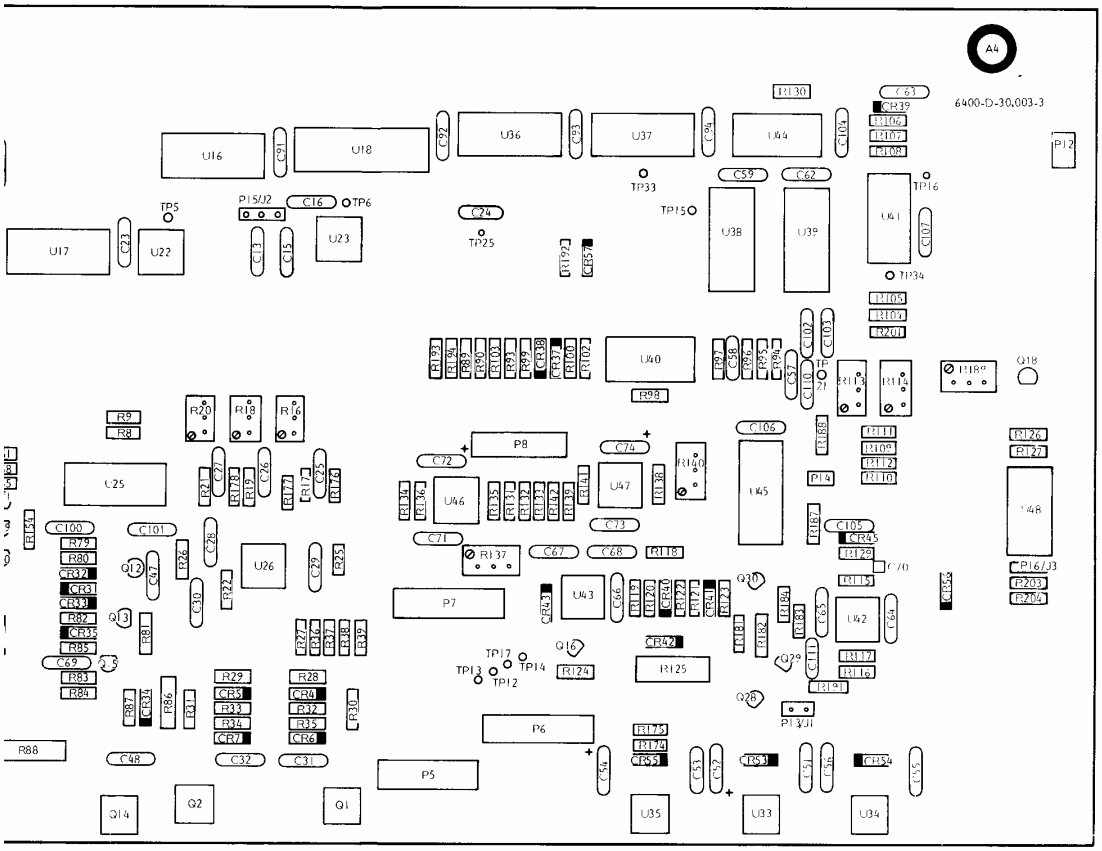
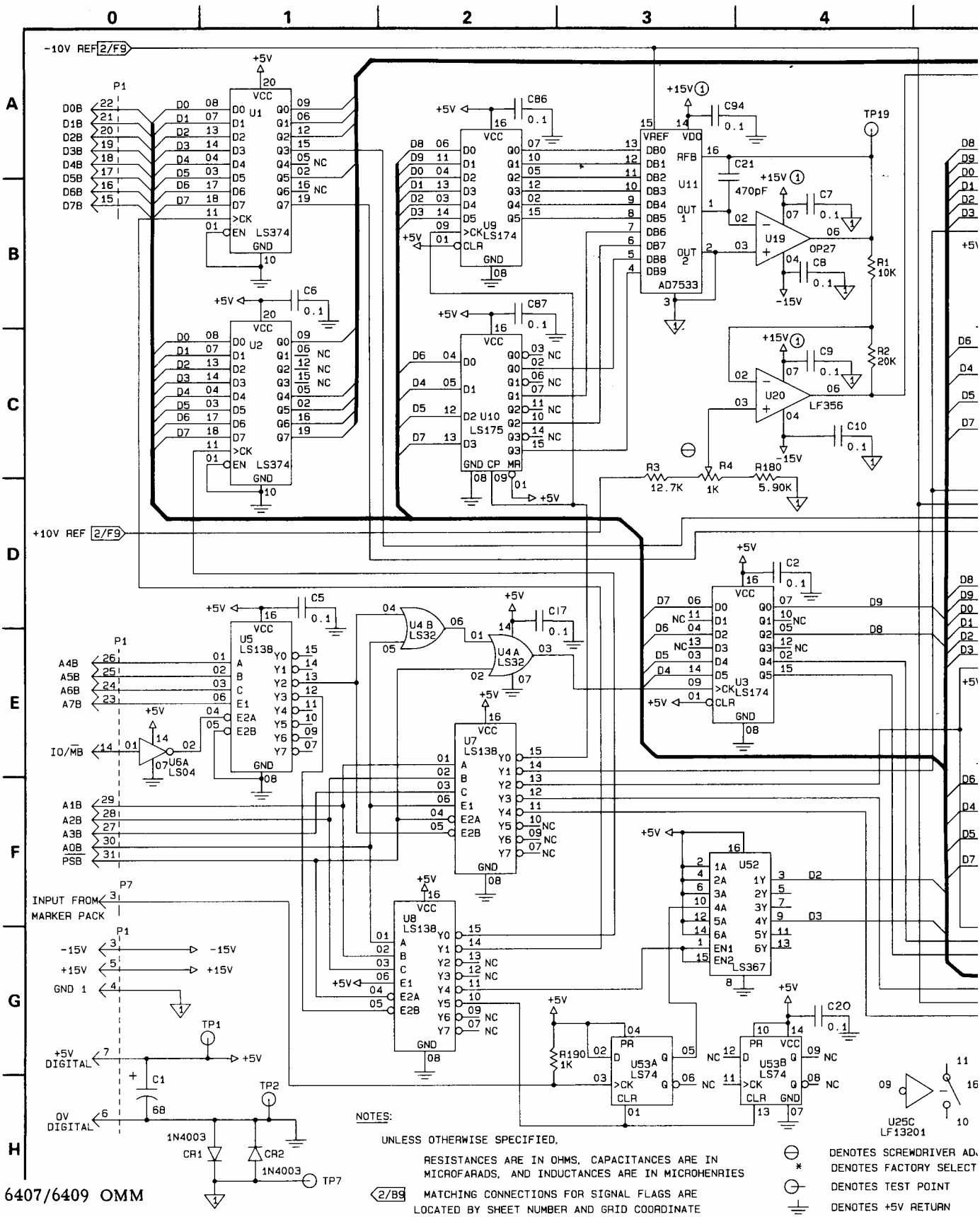
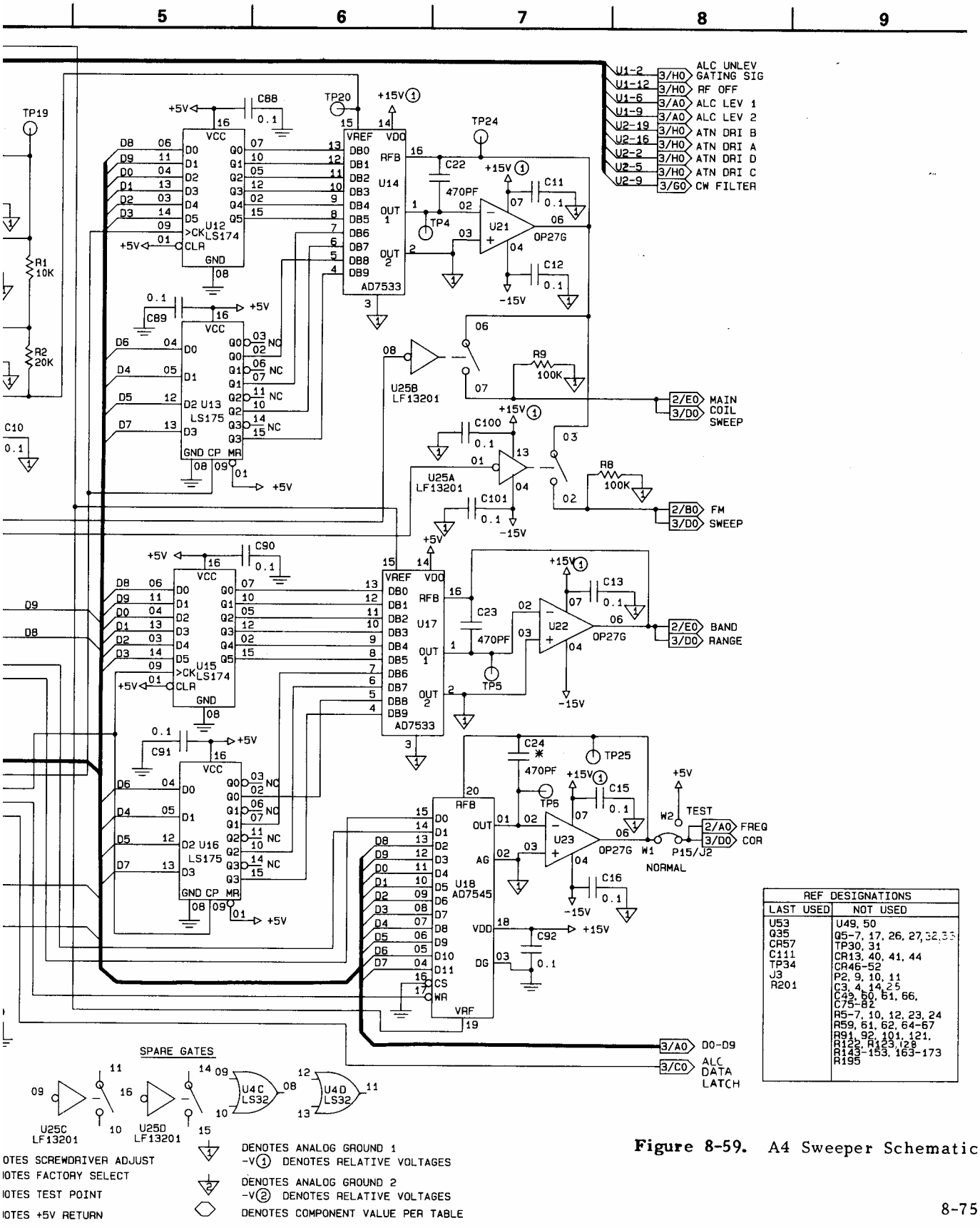


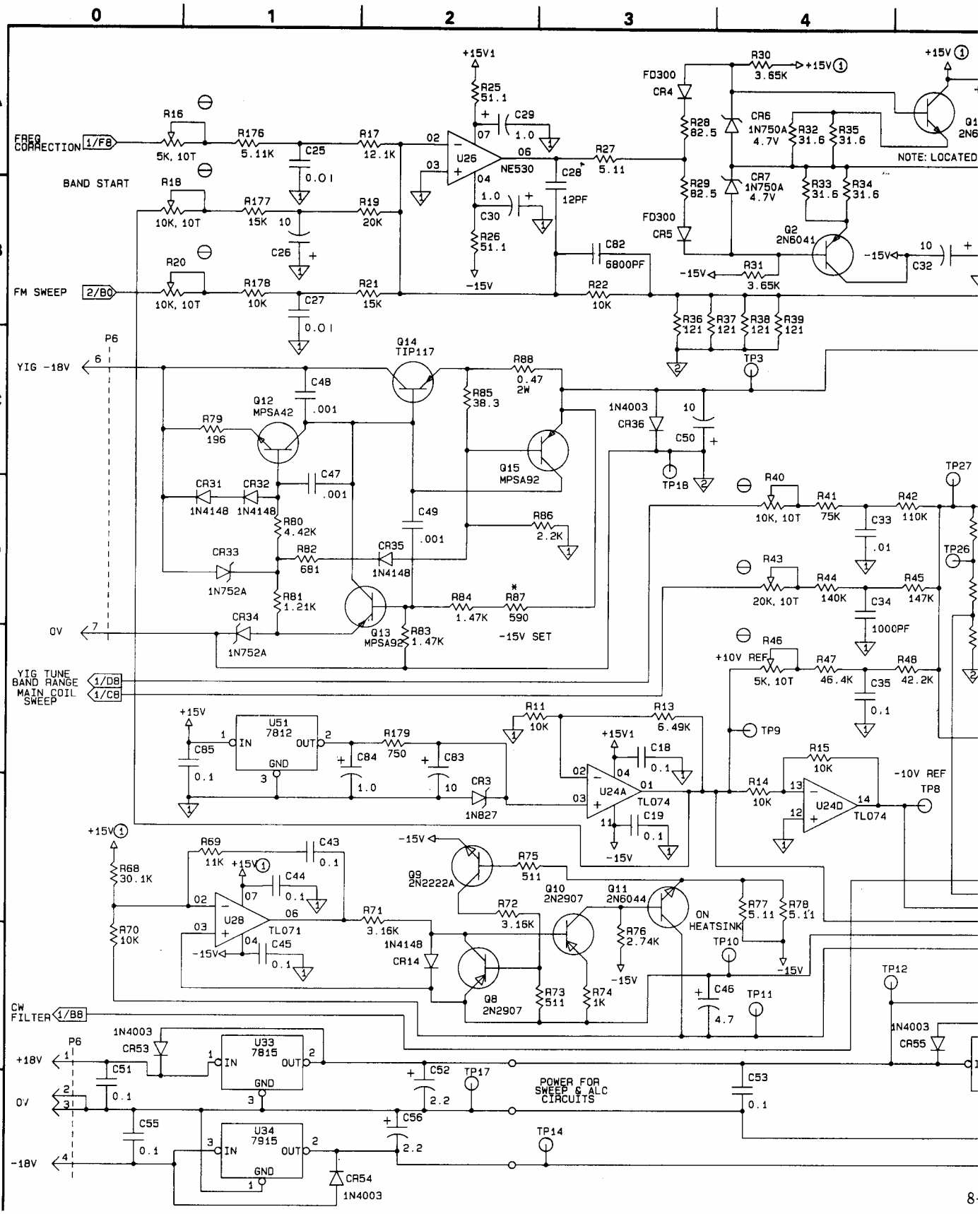
Figure 8-58. A4 PCB Parts Locator Diagram


-10V REF 2/F9
+10V REF 2/F9
P1
U1
U2
U3
U4 B LS32
U4 A LS32
U5 LS138
U6A LS04
U7 LS138
U8 LS138
U9 LS174
U10 LS175
U11
U19 OP27
U20 LF356
U52 LS367
U53A LS74
U53B LS74
U25C LF13201
AD7533
TP19
TP1
TP2
TP7
CR1 1N4003
CR2 1N4003
C1 68
C2 0.1
C5 0.1
C6 0.1
C7 0.1
C8 0.1
C9 0.1
C10 0.1
C17 0.1
C20 0.1
C21 470pF
C86 0.1
C87 0.1
C94 0.1
R1 10K
R2 20K
R3 12.7K
R4 1K
R180 5.90K
R190 1K
+5V
+15V
-15V
+5V DIGITAL
0V DIGITAL
IO/M̄B
A1B
A2B
A3B
A0B
P̄S̄B̄
INPUT FROM MARKER PACK
GND 1
NOTES:
UNLESS OTHERWISE SPECIFIED,
RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS, AND INDUCTANCES ARE IN MICROHENRIES
2/B9 MATCHING CONNECTIONS FOR SIGNAL FLAGS ARE LOCATED BY SHEET NUMBER AND GRID COORDINATE
DENOTES SCREWDRIVER AD
DENOTES FACTORY SELECT
DENOTES TEST POINT
DENOTES +5V RETURN



REF DESIGNATIONS	
LAST USED	NOT USED
U53	U49, 50
Q35	Q5-7, 17, 26, 27, 32, 33
CR57	TP30, 31
C111	CR13, 40, 41, 44
TP34	CR46-52
J3	P2, 9, 10, 11
R201	C3, 4, 14, 25
	C29, 60, 61, 66, C75-82
	R5-7, 10, 12, 23, 24 R59, 61, 62, 64-67 R91, 92, 101, 121, R122, R123, 128 R145-153, 163-173 R195

Figure 8-59. A4 Sweeper Schematic


0
1
2
3
4
A
B
C
D
E
F
G
H
FREQ CORRECTION 1/F8
BAND START
FM SWEEP 2/B0
YIG TUNE 1/D8
BAND RANGE
MAIN COIL SWEEP 1/C8
CW FILTER 1/B8
R16 5K, 10T
R176 5.11K
R17 12.1K
R18 10K, 10T
R177 15K
R19 20K
R20 10K, 10T
R178 10K
R21 15K
C25 0.01
C26
C27 0.01
U26 NE530
+15V1
R25 51.1
R26 51.1
C29 1.0
C30 1.0
C28 12PF
R27 5.11
C82 6800PF
R22 10K
-15V
R30 3.65K
R31 3.65K
FD300 CR4
FD300 CR5
R28 82.5
R29 82.5
CR6 1N750A 4.7V
CR7 1N750A 4.7V
R32 31.6
R33 31.6
R35 31.6
R34 31.6
Q2 2N6041
C32 10
NOTE: LOCATED
R36 121
R37 121
R38 121
R39 121
TP3
P6
YIG -18V
Q14 TIP117
C48 .001
Q12 MPSA42
R79 196
R88 0.47 2W
R85 38.3
Q15 MPSA92
1N4003 CR36
C50 10
TP18
CR31 1N4148
CR32 1N4148
C47 .001
C49 .001
R80 4.42K
R82 681
CR33 1N752A
CR35 1N4148
R81 1.21K
CR34 1N752A
Q13 MPSA92
R83 1.47K
R84 1.47K
R87 590
-15V SET
0V
R40 10K, 10T
R41 75K
R42 110K
C33 .01
TP27
TP26
R43 20K, 10T
R44 140K
R45 147K
C34 1000PF
R46 +10V REF
5K, 10T
R47 46.4K
R48 42.2K
C35 0.1
TP9
U51 7812
C85 0.1
R179 750
C84 1.0
C83 10
CR3 1N827
R11 10K
R13 6.49K
U24A TL074
C18 0.1
C19 0.1
R15 10K
R14 10K
U24D TL074
-10V REF
TP8
R69 11K
C43 0.1
C44 0.1
R68 30.1K
R70 10K
U28 TL071
C45 0.1
R71 3.16K
1N4148 CR14
Q9 2N2222A
R75 511
Q10 2N2907
Q11 2N6044
R72 3.16K
R76 2.74K
ON HEATSINK
R77 5.11
R78 5.11
TP10
Q8 2N2907
R73 511
R74 1K
C46 4.7
TP11
TP12
1N4003 CR55
1N4003 CR53
U33 7815
C51 0.1
C52 2.2
TP17
POWER FOR SWEEP & ALC CIRCUITS
C53 0.1
C55 0.1
U34 7915
C56 2.2
TP14
CR54 1N4003
+18V
0V
-18V

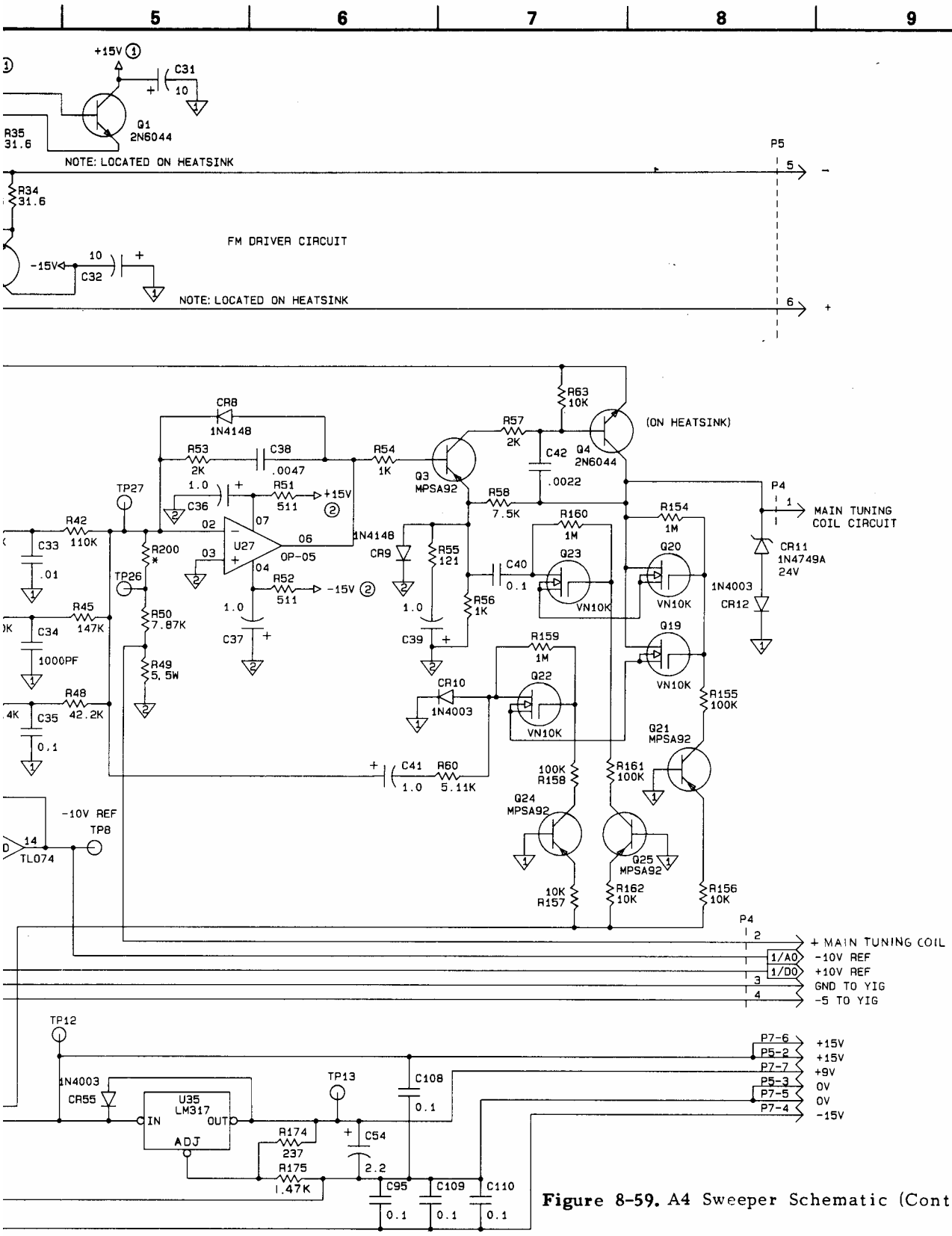
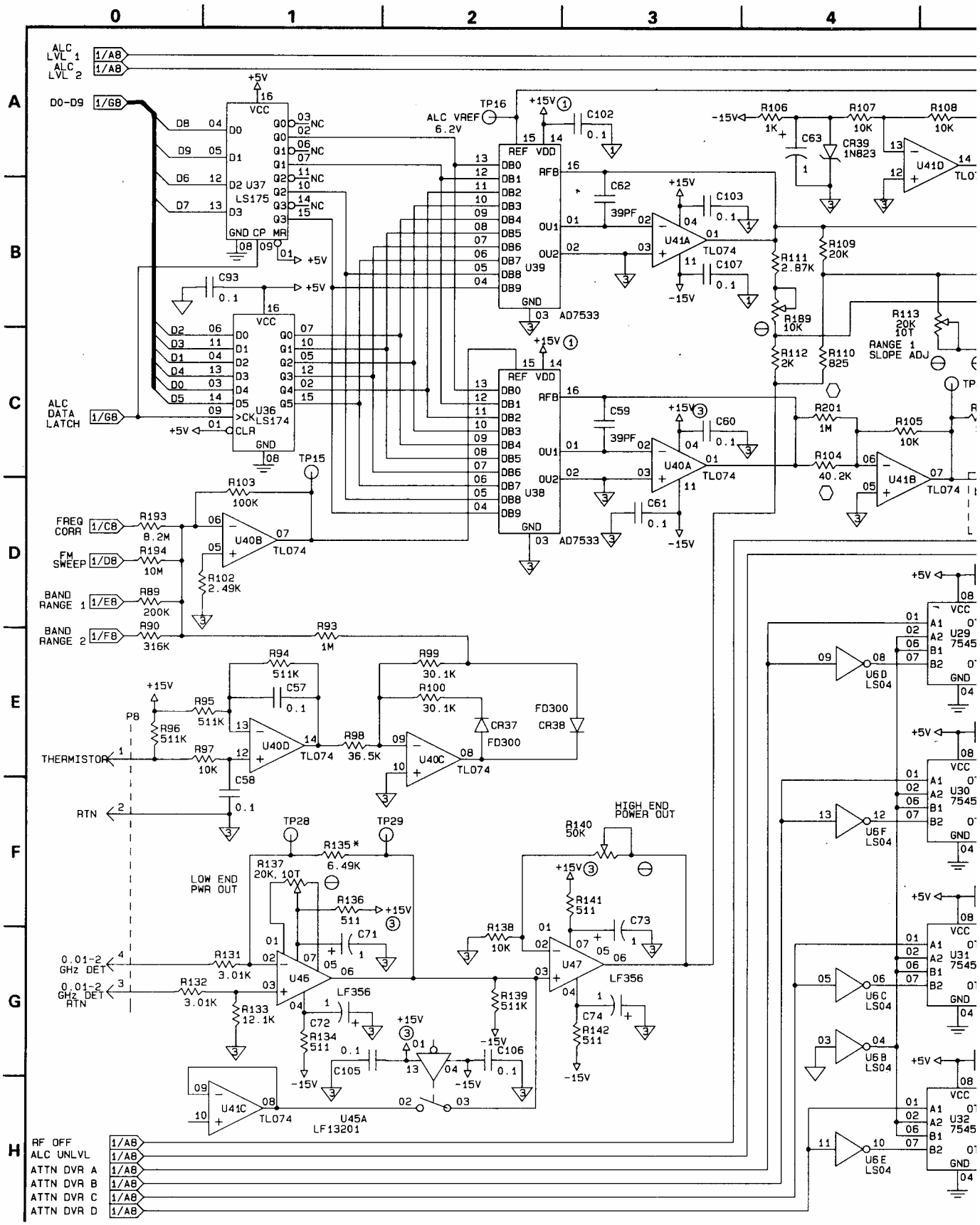


Figure 8-59. A4 Sweeper Schematic (Continued)


0
1
2
3
4
A
B
C
D
E
F
G
H
ALC LVL 1
ALC LVL 2
D0-D9
ALC DATA LATCH
U37 LS175
U36 LS174
U39 AD7533
U38 AD7533
ALC VREF 6.2V
TP16
TP15
TP28
TP29
U41A TL074
U41B TL074
U41C TL074
U41D TL074
U40A TL074
U40B TL074
U40C TL074
U40D TL074
U45A LF13201
U46 LF356
U47 LF356
CR39 1N823
CR37 FD300
CR38 FD300
RANGE 1 SLOPE ADJ
FREQ CORR
FM SWEEP
BAND RANGE 1
BAND RANGE 2
THERMISTOR
RTN
LOW END PWR OUT
HIGH END POWER OUT
0.01-2 GHz DET
0.01-2 GHz DET RTN
U6D LS04
U6F LS04
U6C LS04
U6B LS04
U6E LS04
U29 7545
U30 7545
U31 7545
U32 7545
RF OFF
ALC UNLVL
ATTN DVR A
ATTN DVR B
ATTN DVR C
ATTN DVR D

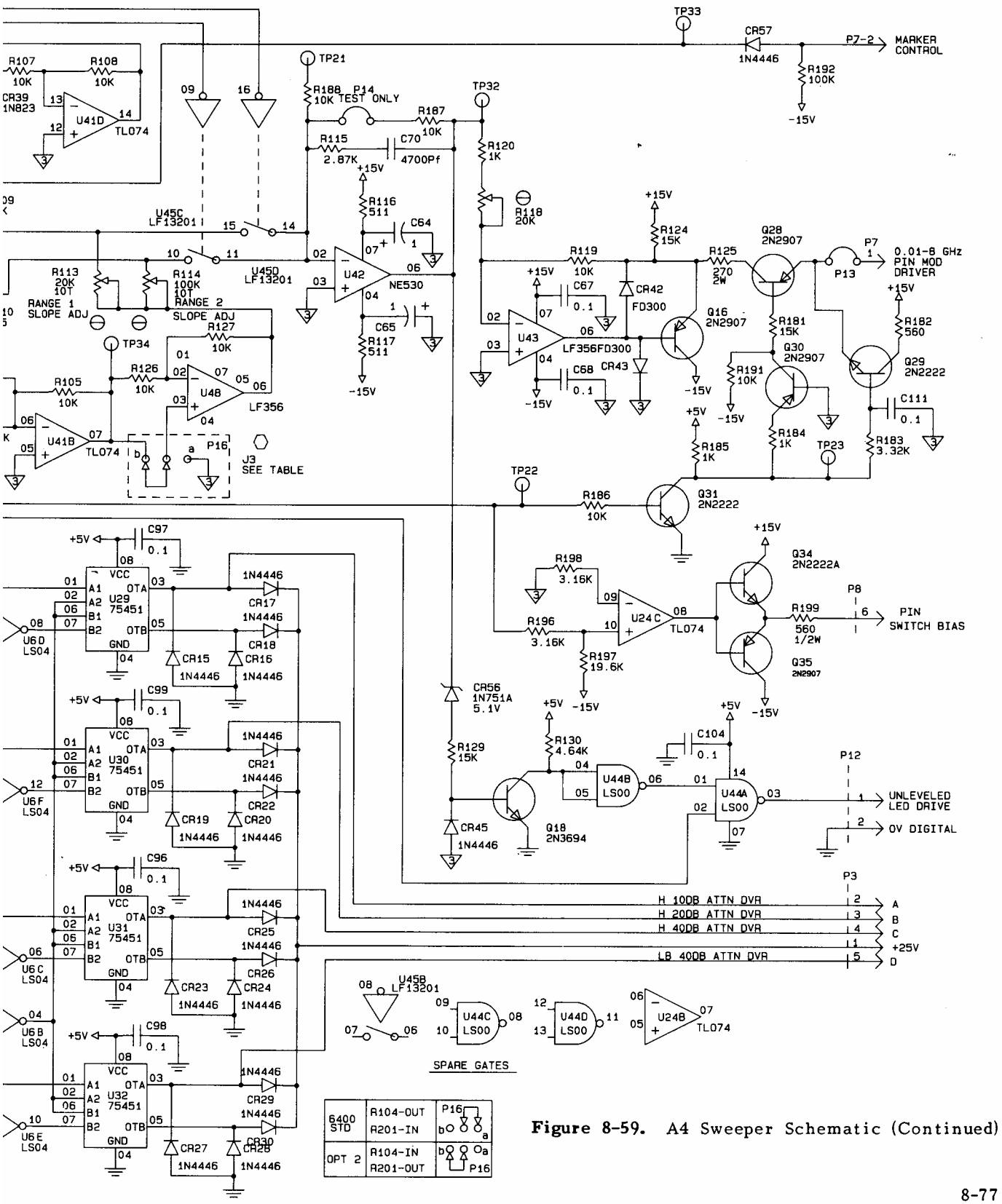


Figure 8-59. A4 Sweeper Schematic (Continued)

8-7.5 RF Components Deck

The RF deck contains the components necessary to generate sweep- and CW-frequency RF signals. The overall RF deck block diagram is shown in Figure 8-60. The RF deck interfaces to the A4 sweeper PCB as shown in Figure 8-61.

a. Oscillator. The YIG oscillator generates swept or CW RF signals.

b. Isolator. The isolator prevents reflected RF energy from returning to the YIG and causing frequency pulling.

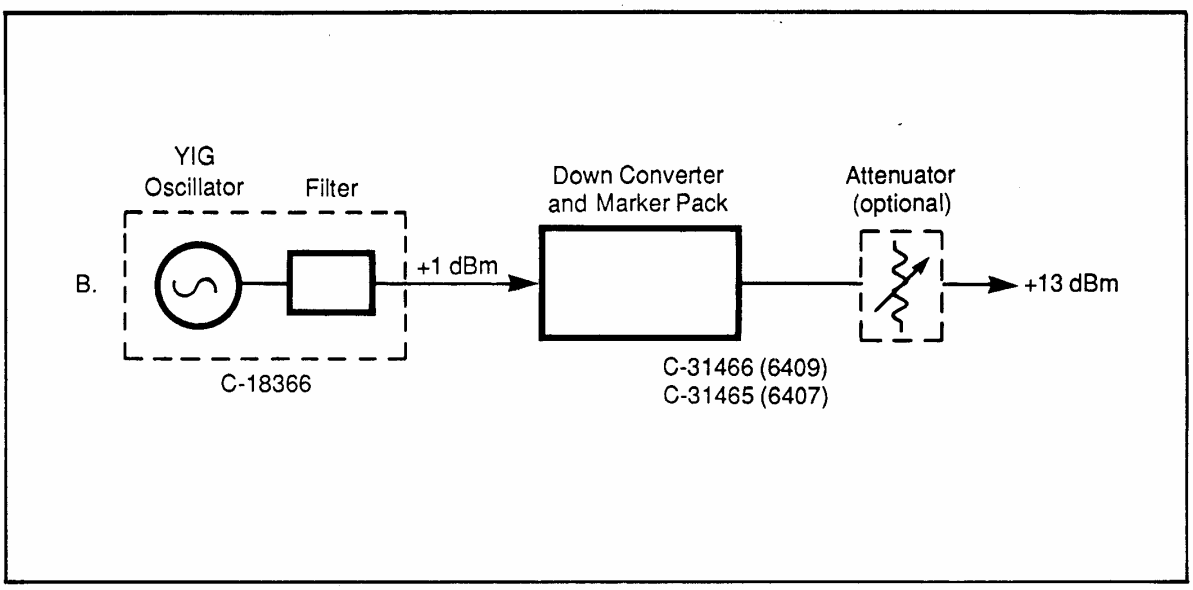


Figure 8-60. RF Components Deck

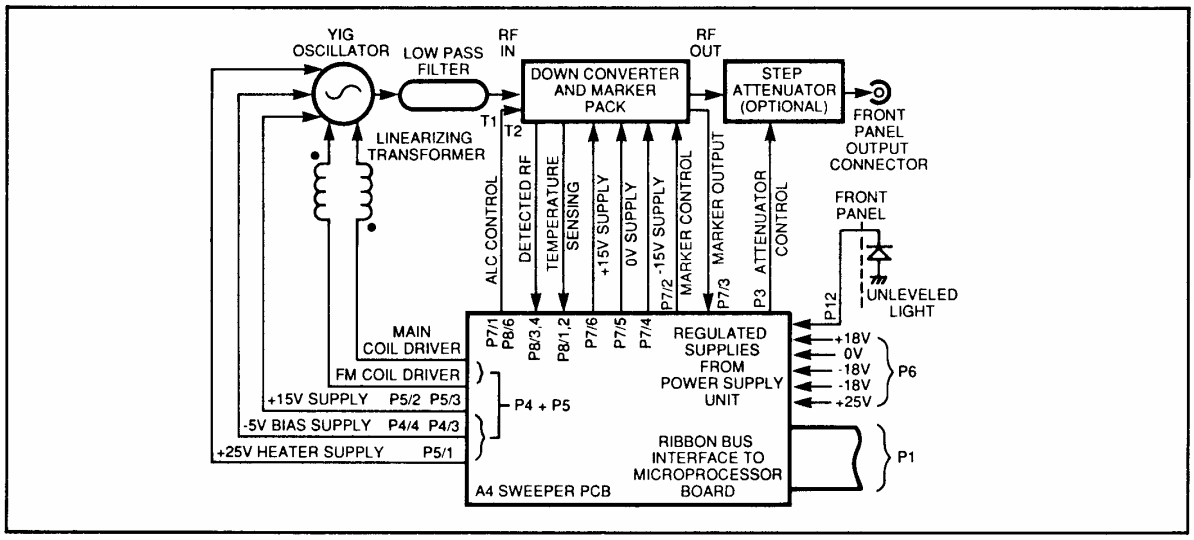


Figure 8-61. RF Deck/A4 PCB Interface

c. Filter. The filter prevents YIG-produced harmonics from mixing with the local oscillator of the down converter.

d. Down Converter and Marker Pack. The down converter produces the correct 6400 operating frequency and the marker pack generates the harmonic comb used to correct swept output frequency.

Also contained in the down converter is a PIN modulator that provides power leveling for the RF output. The PIN modulator is a current-controlled variable attenuator. A simplified schematic of the PIN modulator is shown in Figure 8-62.

e. Attenuator. If fitted, this option provides up to 70 dB of attenuation for the RF output. The drive current for the attenuator is supplied by a cable from the A4 sweep PCB. A simplified attenuator diagram is shown in Figure 8-63.

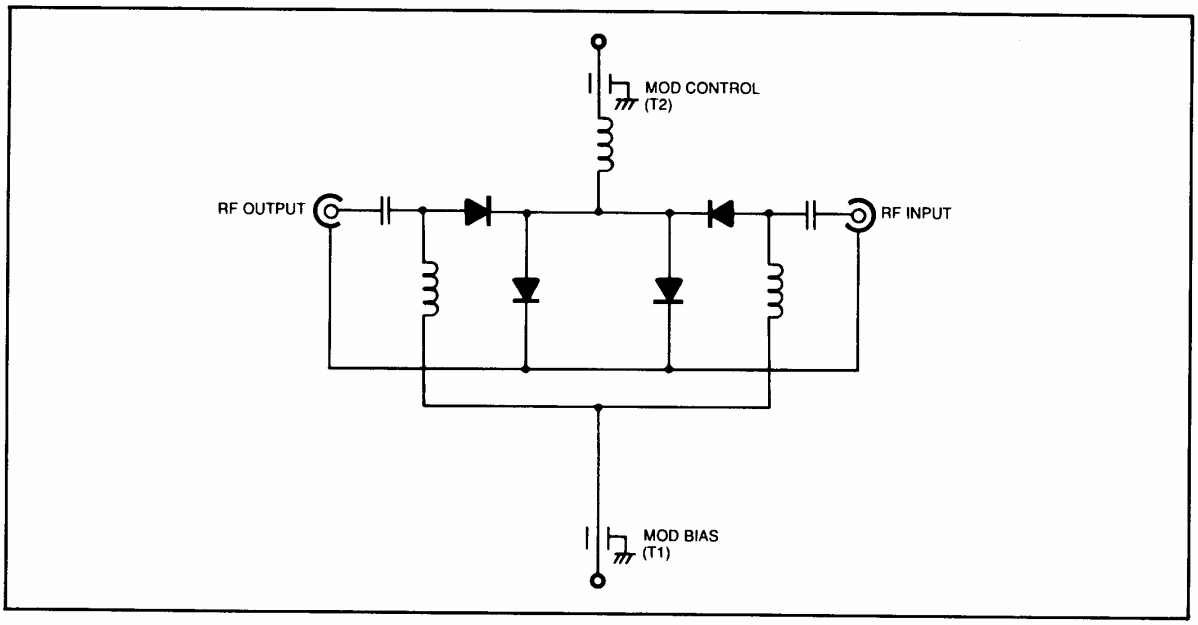
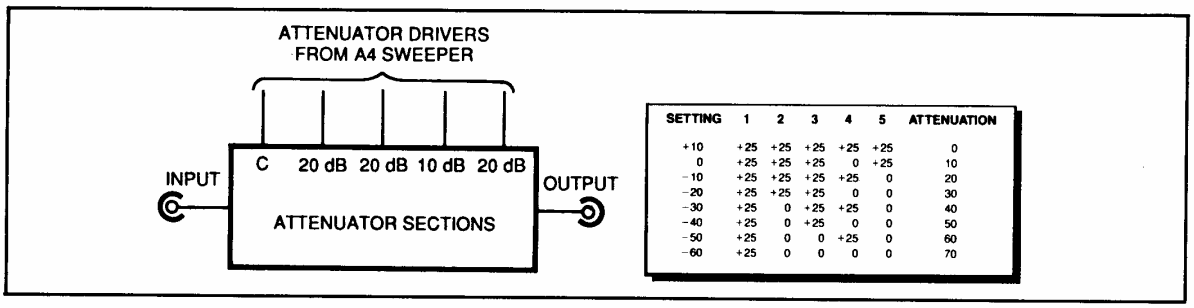


Figure 8-62. PIN Modulator in Down Converter



SETTING	1	2	3	4	5	ATTENUATION
+10	+25	+25	+25	+25	+25	0
0	+25	+25	+25	0	+25	10
−10	+25	+25	+25	+25	0	20
−20	+25	+25	+25	0	0	30
−30	+25	0	+25	+25	0	40
−40	+25	0	+25	0	0	50
−50	+25	0	0	+25	0	60
−60	+25	0	0	0	0	70

Figure 8-63. Attenuator Option

8-7.6 A6 Microprocessor PCB

The A6 microprocessor PCB is the central processing unit (CPU) for the 6400. This section describes the A6 PCB's memory processing functions as well as other functions performed on the A6 board, including:

1. An interrupt interface, which provides support for eight prioritized interrupts.
2. The first stage of the phase-locked loop, which controls the clock for the graphic display processor (GDP) on the A7 PCB.

Figures 8-68, 8-69, and 8-70 show the A6 block diagram, parts locator diagram, and schematic, respectively. Unless otherwise directed, refer to the block diagram for the following discussion.

a. General. The A6 PCB contains the instrument's microprocessor and program memory, including the personality PROM and non-volatile memory. The latter is sustained by a battery backup circuit. The board memory occupies the addresses 0000H to FFFFH (64k) in 8k blocks. Higher addresses are not decoded and overlay the first 64k. For example, an attempt to access address 10000H will actually access address 0000H.

   A troubleshooting function is provided to isolate the microprocessor from all memory so that data lines can be analyzed. A 16-pin DIL test header can force the data bus to contain a one byte instruction at all times. This frees the microprocessor from memory contents and addressing integrity.

   All instrument PCBs interface to the microprocessor through ports. To minimize hardware on each board, block decoding of the ports is performed on the A6 PCB. Eight In/Out select lines ($\overline{IOSEL_0}$ thru $\overline{IOSEL_7}$) are sent out from A6. Each line pulses LOW when data is provided or expected from a port in the range of that line. Not all of these ports are used.

b. Clock. The microprocessor, U1, runs at a frequency determined by crystal X1. This crystal forms a simple oscillator with U2. The output of the circuit is the crystal frequency divided by three.

   The Power-on Reset is formed by R1, CR4, and C1 and has a time constant of one second. CR4 provides a rapid discharge path for C1, ensuring that a reset occurs in the event of brief power losses.

   The clock shape and time period can be measured at TP1. The clock is buffered for external use by U12A. This output appears at P8, pin M. This clock output is used by the A8 GPIB board, if the GPIB option is installed.

   Because of the long interface length to some PCBs, one wait-state is provided for all port accesses (to external boards) by U24 and U10C and D. This extra clock cycle, or wait-state, compensates for the slower exchange of control signals and data. One clock cycle is inserted in the read or write line when the In/Out/$\overline{Memory}$ (IO/$\overline{M}$) signal is HIGH, as it is for port activity.

c. Address and Memory. The low order address lines, A_0 thru A_7, are multiplexed with the data lines. These lines are separated by U4, which latches in the address lines using the Address Latch Enable (ALE) lines on U1 (pin 25). The address lines are buffered to the rest of the board through U4, and to the rest of the instrument through U11.

   The unseparated data bus, AD_0 thru AD_{12}, is taken directly to all the EPROMs and RAM, U13 thru U20, through the 16 pin DIL test header. In normal use, the test header connects across the eight data lines. For test purposes, a header can be installed that pulls the data

Table 8-11. A6 Memory Map

Block Address	U#	Memory	Type
0000H-1FFFH	U13	2764	8K EPROM
2000H-3FFFH	U14	2764	8K EPROM
4000H-5FFFH	U15	2764	8K EPROM
6000H-7FFFH	U16	2764	8K EPROM
8000H-9FFFH	U17	6264LP	8K CMOS RAM
A000H-BFFFH	U18	6264LP	8K CMOS RAM
C000H-DFFFH	U19	2764	8K EPROM
E000H-FFFFH	U20	2764	8K EPROM (personality)

lines to a preset value corresponding to a one byte instruction for U1. This makes the microprocessor free run through all the address space so that address lines can be checked and verified.

The A6 Memory Map is shown in Table 8-11. Access to the memory chips is standard design. Each chip has a separate block select line that is provided by U5. U5 decodes lines A_{13} through A_{15} from U1 into 8k blocks of memory.

The output enable of each of the memory chips is controlled by the READ line ($\overline{RD}$) from U1. The two RAM chips, U17 and U18, also use a separate supply line and chip select to allow the battery backup function to save the contents of the RAMs in case of failure of the primary power source.

d. Buffering. The data bus is buffered to the rest of the instrument by U9, a bidirectional buffer. The direction of drive is controlled by the buffered U1 $\overline{RD}$ line, and is enabled only during port accesses. This buffering ensures no bus conflict on the A6 PCB, since all ports are external to this board and no memory exists off the board. (The tick control port, discussed later, is part of the board, but is external to the buffers.) When the buffer is not enabled, the external data bus contents are not defined.

The low order address lines are buffered to the rest of the instrument by U11, which allows further decoding of the port blocks. These lines are also valid during a port access, but are undefined at other times.

Port block decoding is accomplished by U7, which provides eight lines, $\overline{IOSEL_0}$ through $\overline{IOSEL_7}$. The port block description is shown in Table 8-12.

All port block select lines are active LOW. The sweeper control board (A4) decodes its own port selects in the range 80H to BFH. The signals required to do this are buffered by U8 and comprise IO/$\overline{M}$ (In/Out/$\overline{Memory}$), $\overline{WR}$ (Write), $\overline{PSB}$ (Port Strobe) and $\overline{RD}$ (Read). These lines are LOW to indicate Memory access, Write, Port Strobe, and Read respectively. The $\overline{PSB}$ line is $\overline{RD}$ or $\overline{WR}$ gated with IO/$\overline{M}$ and is LOW during any port access. These lines are active for periods of less that 1 μS at a time.

e. Interrupts. There are eight interrupts supported by the A6 PCB. An interrupt is generated if any one of

Table 8-12. Port Block Description

Port Block	Name	Used On	PCB
00H - 0FH	$\overline{IOSEL_0}$	Signal Channel	A3
10H - 1FH	$\overline{IOSEL_1}$	Signal Channel	A3
20H - 2FH	$\overline{IOSEL_2}$	Control Panel	A1
30H - 3FH	$\overline{IOSEL_3}$	(not used)	--
40H - 4FH	$\overline{IOSEL_4}$	CPU (Tick)	A6
50H - 5FH	$\overline{IOSEL_5}$	GPIB/Centronics	A10
60H - 6FH	$\overline{IOSEL_6}$	GDP	A7
70H - 7FH	$\overline{IOSEL_7}$	(not used)	--

lines $\overline{INT_0}$ to $\overline{INT_7}$ is LOW. These lines are encoded in priority by U23, with $\overline{INT_0}$ having the highest priority. Three bits from U22, together with the enable line from U23 (pin 15), are buffered onto the data bus when enabled by the interrupt-acknowledge line ($\overline{INTA}$) from U1. This forces the microprocessor to perform a special routine for the active interrupt.

f. Battery Backup. The battery backup circuit saves the contents of the RAMs when the primary power source fails. This circuitry is divided into two sections: µP control and RAM control.

1. µP Control. This section stops the µP from making any further memory accesses when a power failure is detected on the 5V rail. It consists of micropower comparator U28, transistor Q5, and associated components (Figure 8-64).

Micropower comparator U28 senses a threshold voltage that is set by resistor chain R24, R29, R25, and R26. Normally, when the supply voltage is above the threshold level, transistor Q5 is turned off and the $\overline{RESET}$ input of U2 is held to a logic HIGH by R1 and C1.

When the supply voltage falls below the threshold value, Q5 turns on, discharging C1 and pulling $\overline{RESET}$ to logic LOW, thus inhibiting the RIN pin on U2. R28 provides current limiting and R27 provides sufficient base drive current to ensure that Q5 turns on properly.

2. RAM Control. This section, upon detecting a power failure, supplies an inhibit signal and a reduced, battery-supplied voltage to the RAMs. It consists of microcomparator U21, transistors Q1 thru Q4 and associated components (Figure 8-65).

Micropower comparator, U21, senses a threshold voltage set by resistor chain R7, R30, R8, and R9. Normally, when the supply is above the threshold voltage, transistor Q4 is turned off. The $\overline{CMOS\ STDBY}$ line is HIGH, enabling the RAMs, and turning on Q2 and Q3.

These two transistors then turn on transistor Q1, which connects the main 5V supply rail to the RAM chips, and trickle charges the battery through R13.

When the supply voltage falls below the threshold value, Q4

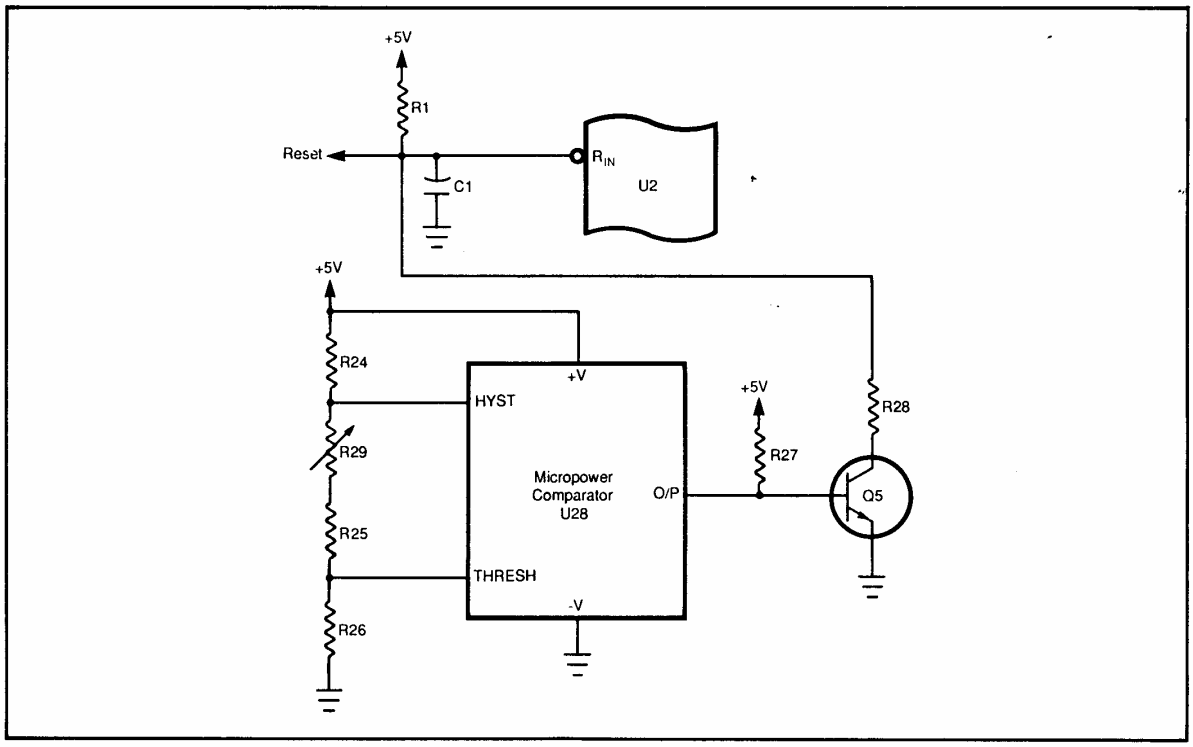


Figure 8-64. Microprocessor Control Circuit

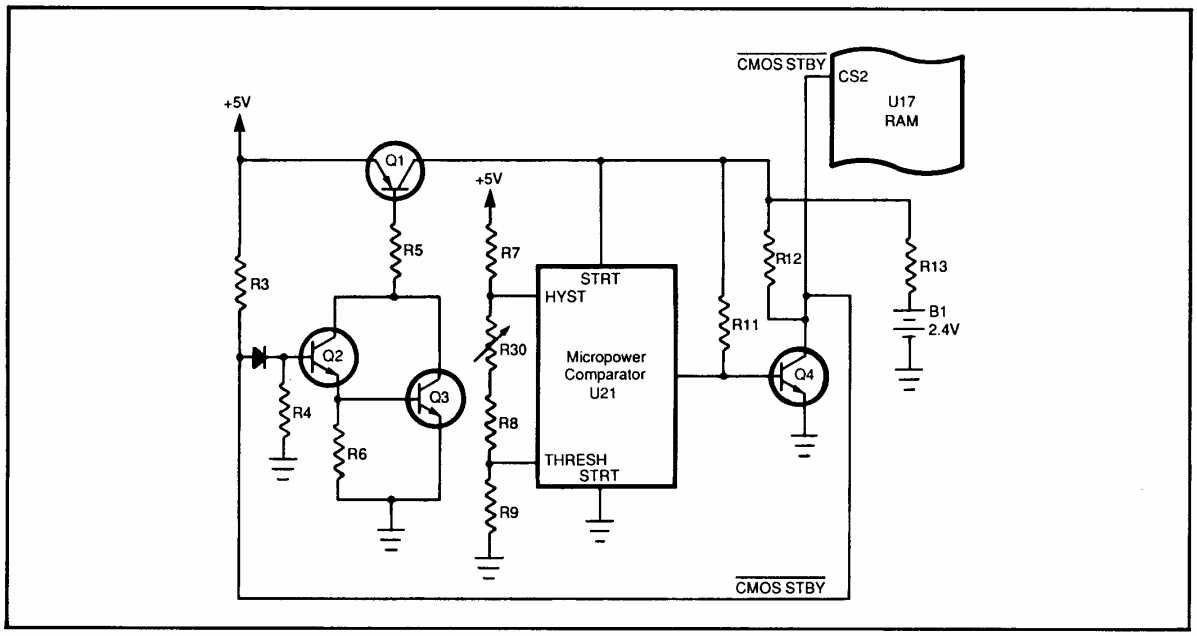


Figure 8-65. RAM Control Circuit

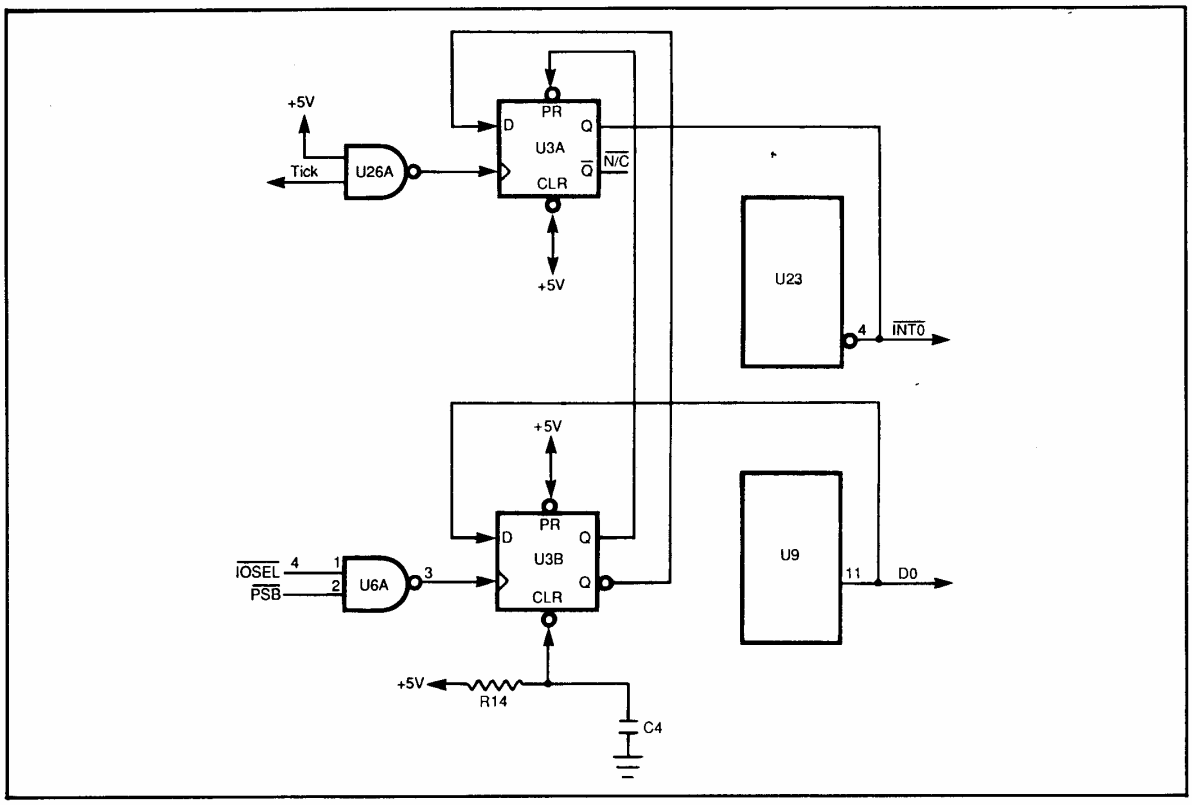


Figure 8-66. Line Interrupt Circuit

turns on. The CMOS STDBY line is pulled LOW, inhibiting the RAMs and turning off Q2 and Q3. This action turns Q1 off, isolating the RAM chips from the main 5V supply rail.

Standby current, at a reduced voltage, is then supplied to the RAMs from the battery. Resistors R4, R5, R6, R11, and R12 provide biasing for the transistors in this section.

g. Line Interrupt. The line interrupt circuit enables the microprocessor to schedule operations with reference to a real time stimulus, or tick signal. This squarewave tick is obtained from one of the secondary windings on the power supply transformer. The line interrupt circuit consists of U3A, U3B, U6A, and associated components. A simplified schematic is shown in Figure 8-66.

The two major components of this circuit are the interrupt latch, U3A, and the control latch, U3B. When the U3B control latch is set (Q output HIGH), any rising edge of the tick signal sets U3B to its active state. The $\overline{INT_0}$ is then held LOW. The circuit will remain in this stable state, with the interrupt active (regardless of what happens at the tick input), until the microprocessor clears the condition. The clearing is done by resetting the U3B control latch to both clear and disable the interrupt, then setting it again to re-enable the latch. The latch is now ready for the next rising edge of the tick signal.

To set the U3B control latch, the microprocessor writes a data byte to port 40H, with data bit D0 set to 1. This enables the U3A interrupt latch.

To reset the U3B control latch, the microprocessor writes a data byte to port 40H with data bit D0 set to 0. This disables the U3A interrupt latch and resets the $\overline{INT_0}$ line to its inactive state. On initial power ON, R14 and C4 perform a hardware reset to the U3B control latch.

h. Phase Lock Loop Circuitry. This circuitry, in conjunction with other circuitry on the A7 PCB, controls the frequency of the voltage-controlled oscillator (VCO) A7U3. The phase-lock loop (PLL) circuit consists of U25A, U25B, U26C, U27 and associated circuitry.

The two J-K flip flops U25A and U25B (Figure 8-67) are used as a phase/frequency comparator. The comparison is between the $\overline{VSYNC}$ signal form the Graphics Display Processor on A7 and the line frequency (provided by the tick signal). The signal at the junction of R17 and R18 is a mixture of the two Q outputs of the comparator. When the $\overline{VSYNC}$ signal is in phase with the tick signal, the pulse train at this junction has a mean value of 2V. This value is half way between TTL1 and TTL0. The output of U27 stabilizes as the integrator R19 and C27 smooths the signal to its mean value.

If the inputs are out of phase, the voltages vary in such a way as to cause the output of U27 to move in a direction that will ultimately bring the two input signals back in phase.

i. Links. Three links are provided in the circuit. Links 1 and 2 are hard-wired and no longer used. Link 3 allows isolation of the battery when the A6 PCB is in long term storage. The current drawn from the battery during standby mode is, typically, less than 100µA.

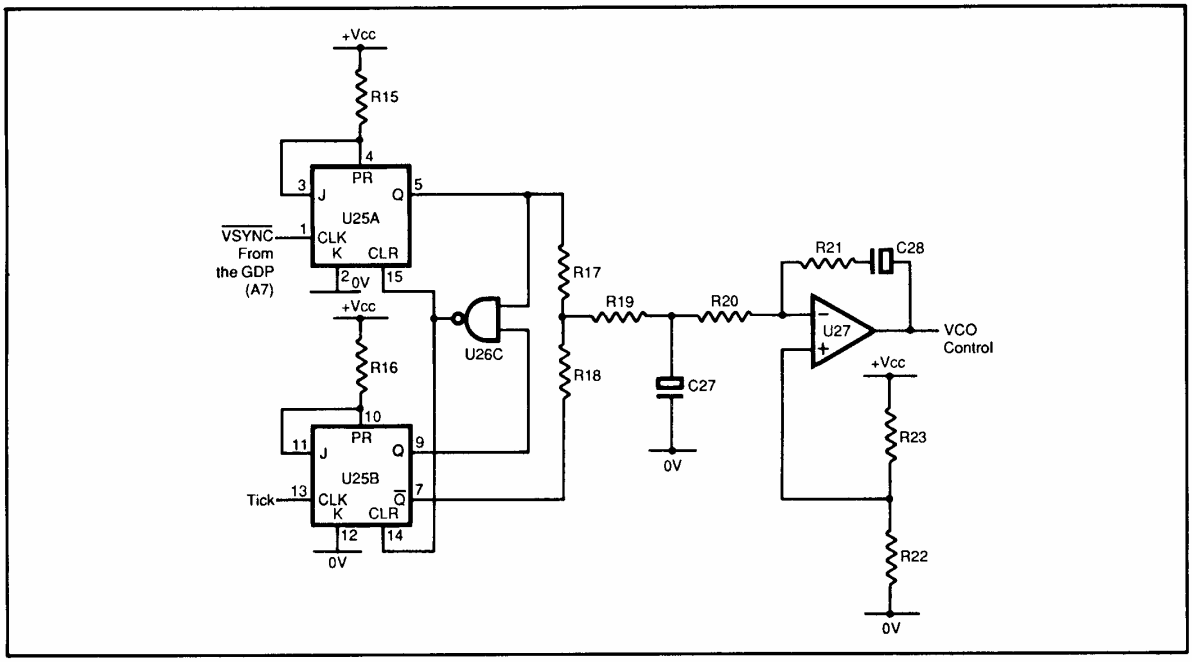
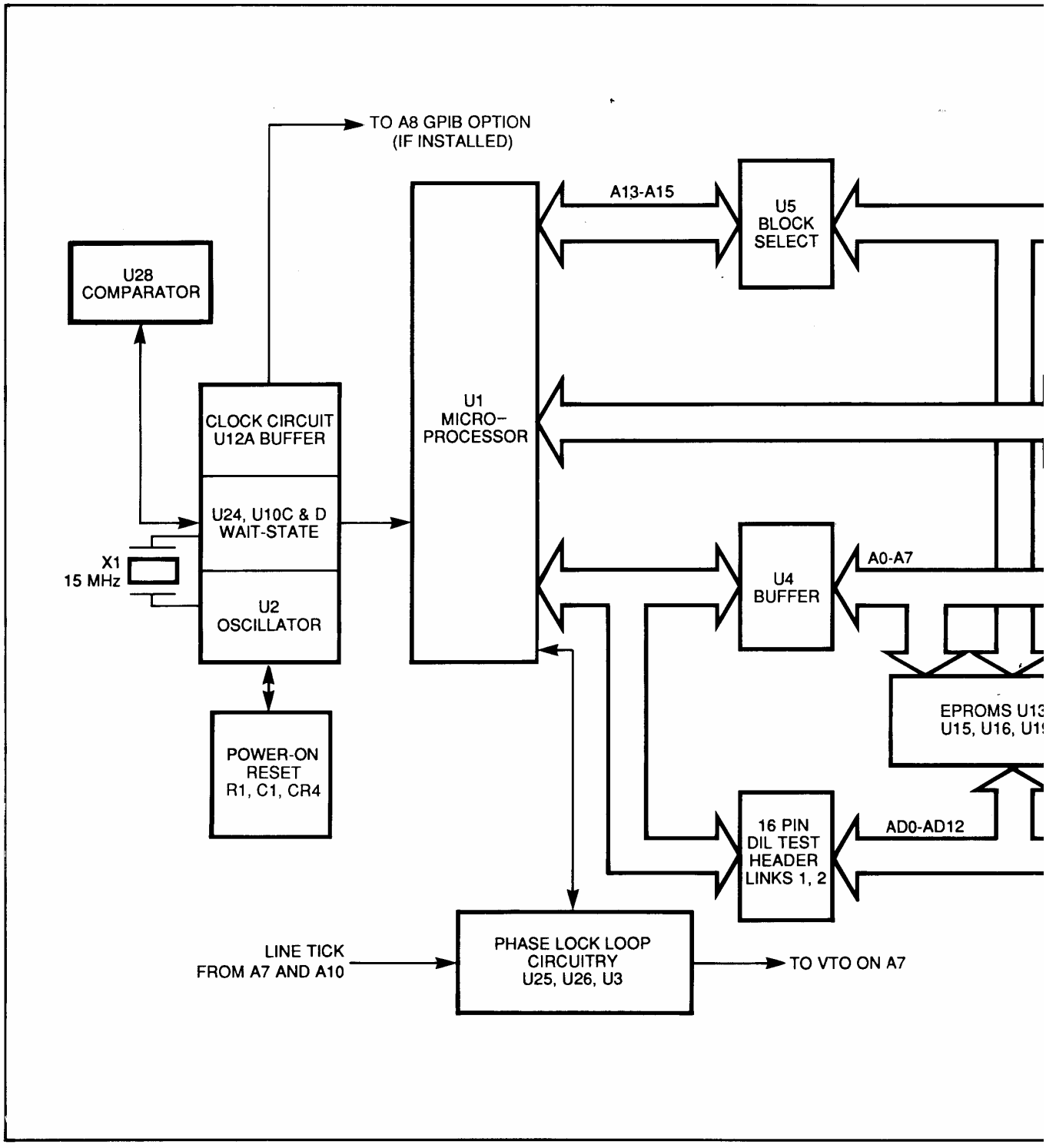


Figure 8-67. Phase-Lock Loop (PLL) Circuit


TO A8 GPIB OPTION
(IF INSTALLED)
U28
COMPARATOR
CLOCK CIRCUIT
U12A BUFFER
U24, U10C & D
WAIT-STATE
U2
OSCILLATOR
X1
15 MHz
POWER-ON
RESET
R1, C1, CR4
U1
MICRO-
PROCESSOR
A13-A15
U5
BLOCK
SELECT
U4
BUFFER
A0-A7
EPROMS U13
U15, U16, U1
16 PIN
DIL TEST
HEADER
LINKS 1, 2
AD0-AD12
LINE TICK
FROM A7 AND A10
PHASE LOCK LOOP
CIRCUITRY
U25, U26, U3
TO VTO ON A7

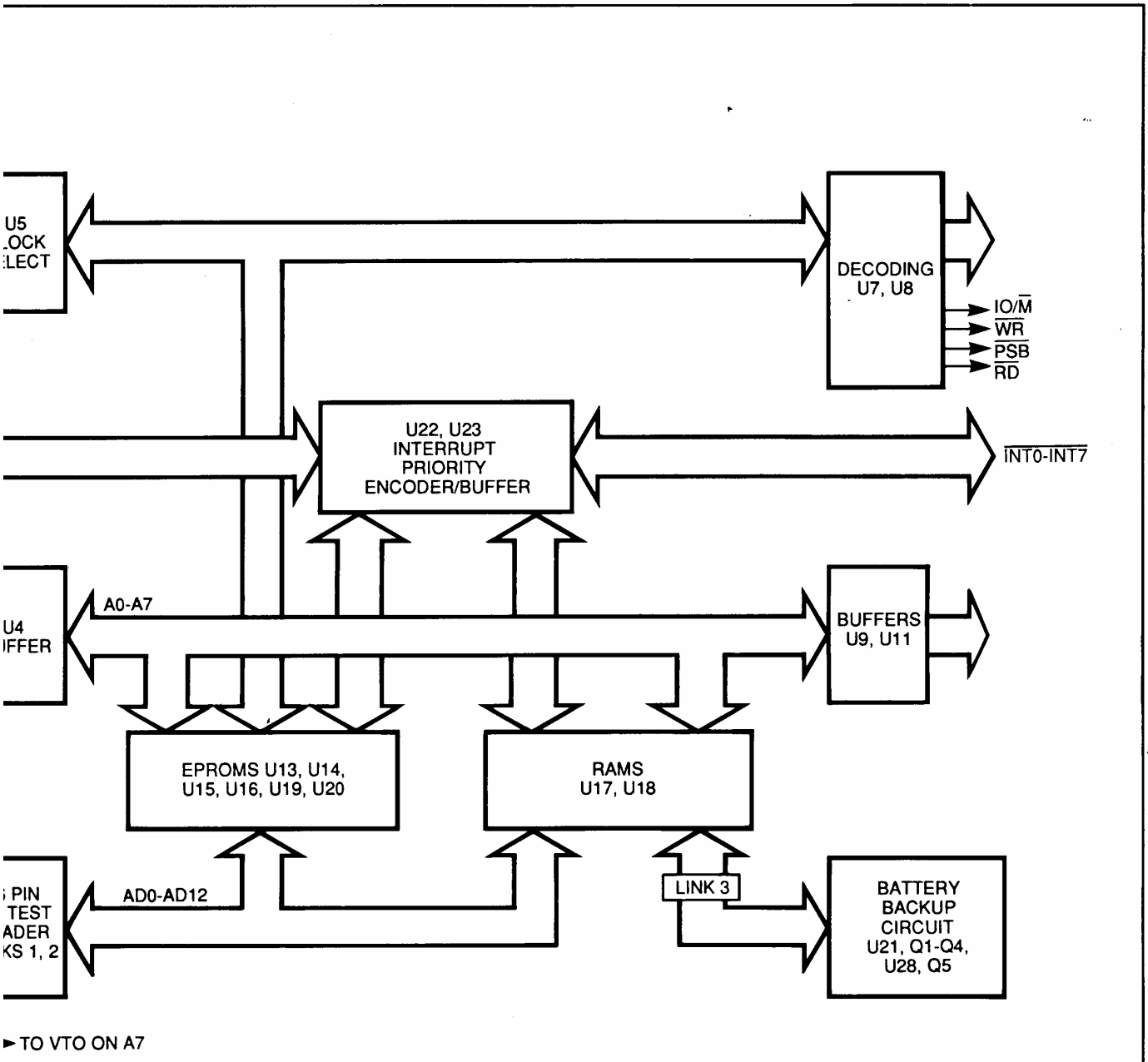


Figure 8-68. A6 CPU Block Diagram

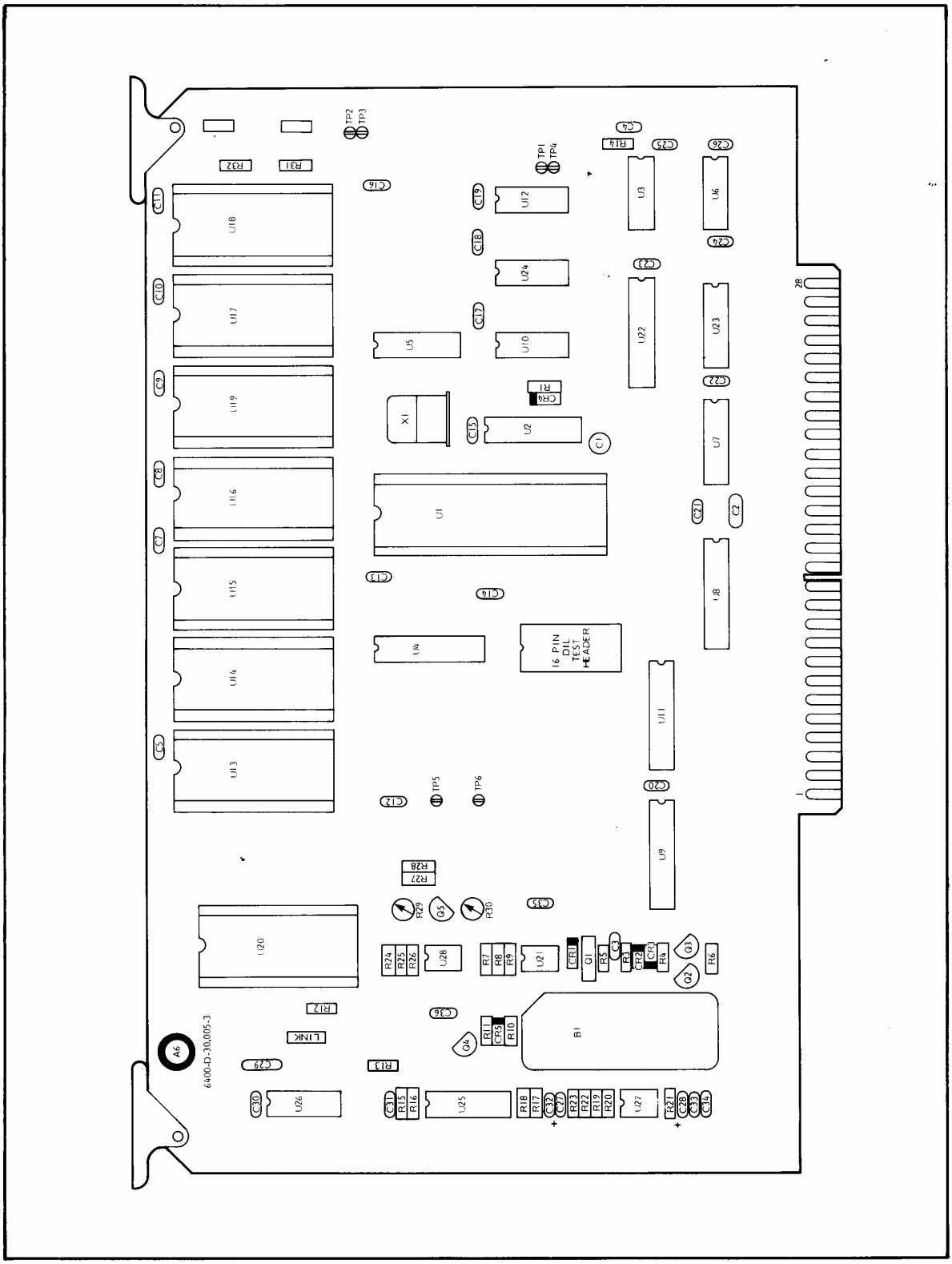
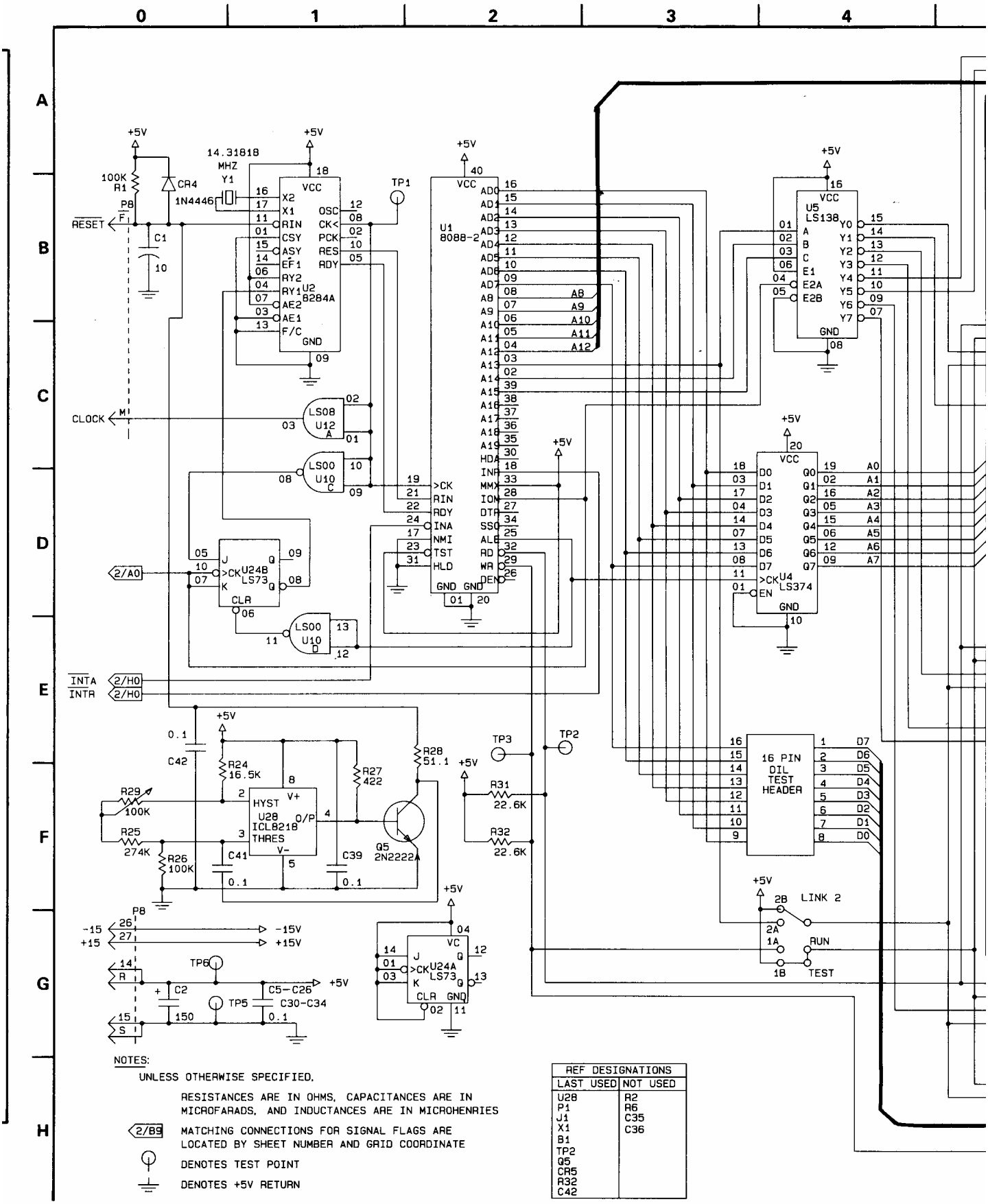


Figure 8-69. A6 PCB Parts Locator Diagram



REF DESIGNATIONS	
LAST USED	NOT USED
U28	R2
P1	R6
J1	C35
X1	C36
B1	
TP2	
Q5	
CR5	
R32	
C42	

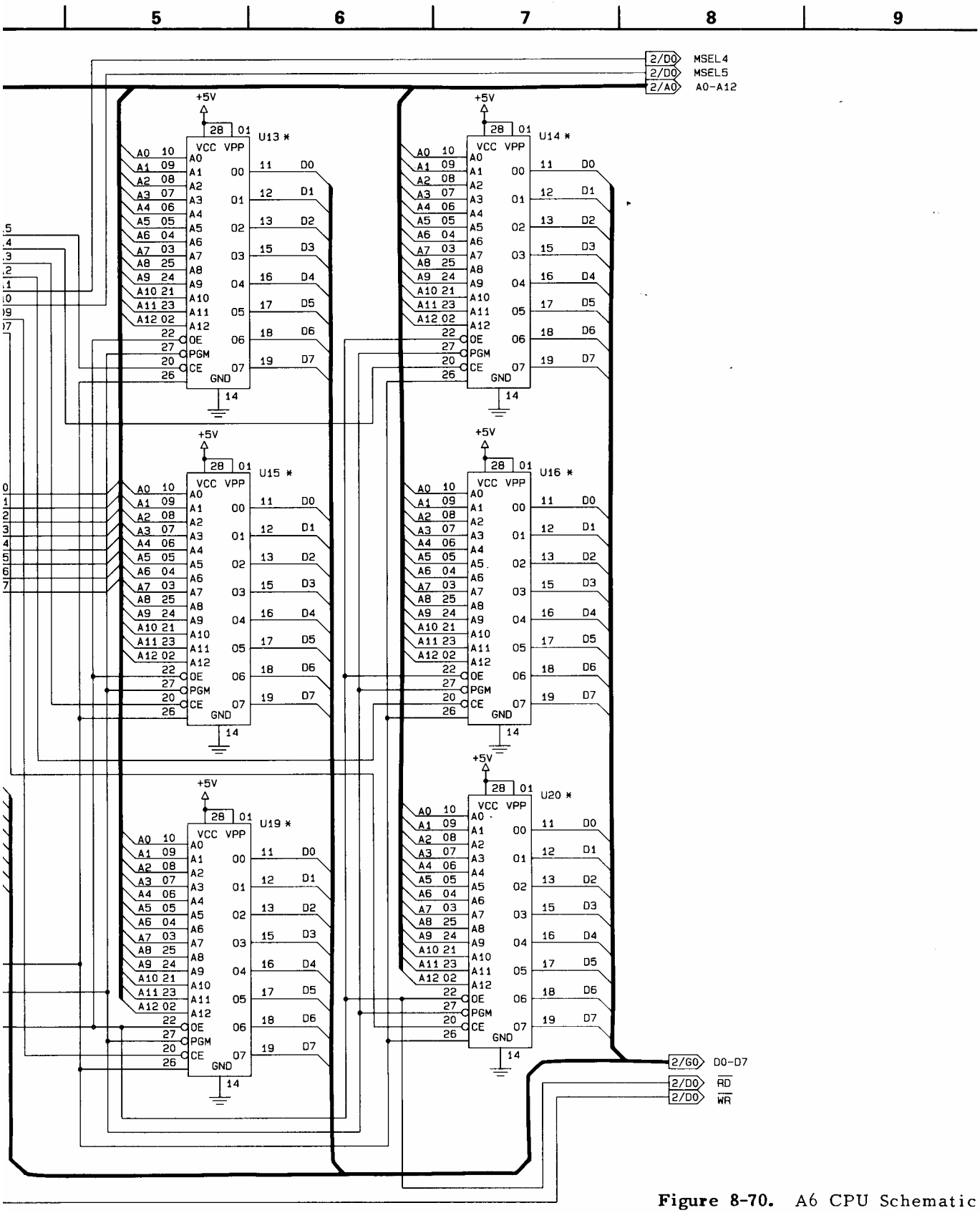
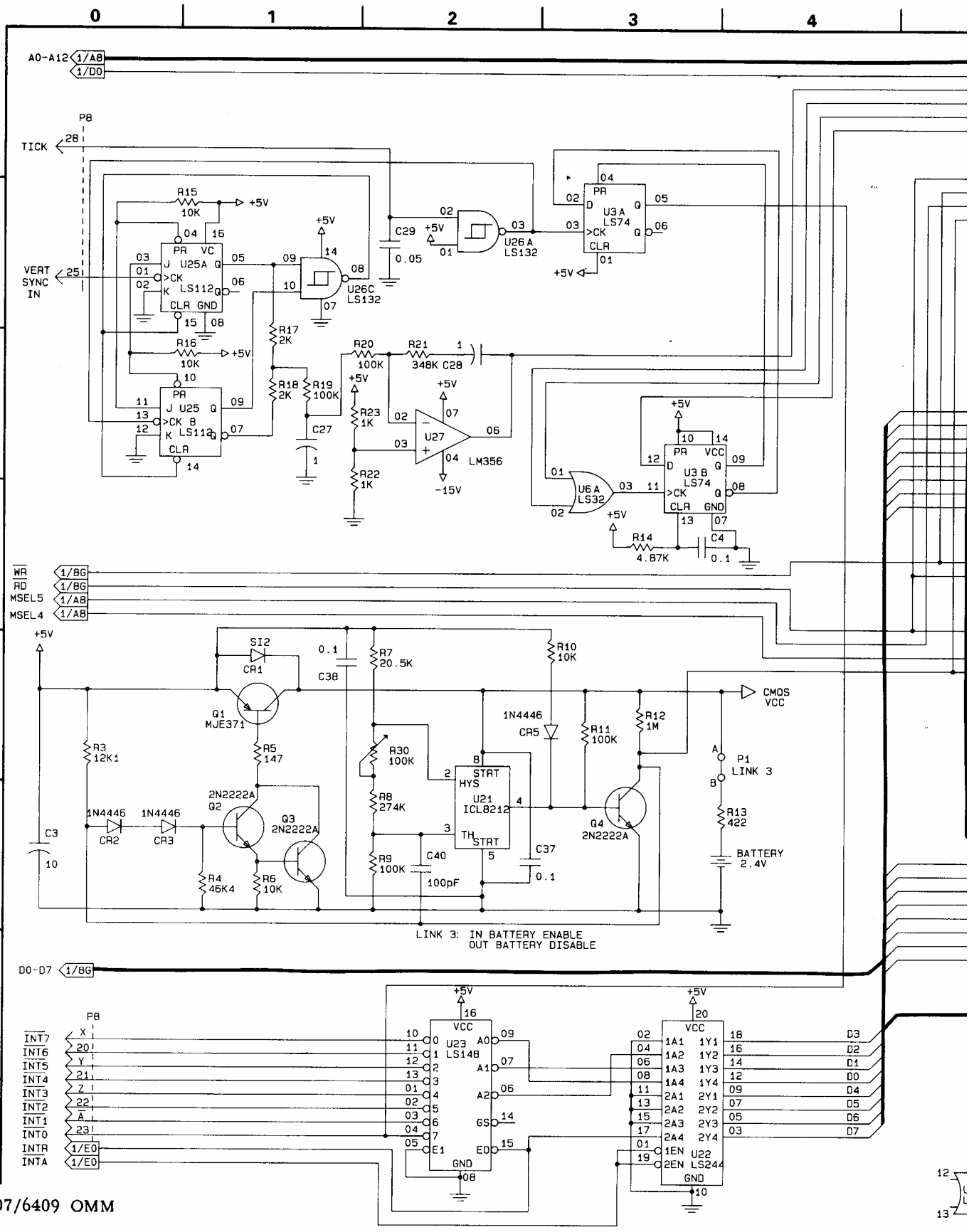


Figure 8-70. A6 CPU Schematic


0
1
2
3
4
A
B
C
D
E
F
G
H
A0-A12 1/A8
1/D0
P8
TICK 28
VERT SYNC IN 25
R15 10K
+5V
U25A LS112
U26C LS132
C29 0.05
U26A LS132
U3A LS74
R16 10K
U25 LS112
R17 2K
R18 2K
R19 100K
C27
R20 100K
R21 348K
C28
R23 1K
R22 1K
U27 LM356
-15V
U6A LS32
U3B LS74
R14 4.87K
C4 0.1
WR 1/8G
RD 1/8G
MSEL5 1/A8
MSEL4 1/A8
SI2
CR1
C38 0.1
R7 20.5K
R10 10K
Q1 MJE371
R3 12K1
R5 147
R30 100K
1N4446
CR5
R11 100K
R12 1M
CMOS VCC
P1 LINK 3
R8 274K
U21 ICL8212
STAT HYS
TH
STAT
2N2222A Q2
Q3 2N2222A
Q4 2N2222A
1N4446 CR2
1N4446 CR3
C3 10
R4 46K4
R6 10K
R9 100K
C40 100pF
C37 0.1
R13 422
BATTERY 2.4V
LINK 3: IN BATTERY ENABLE
OUT BATTERY DISABLE
D0-D7 1/8G
P8
INT7
INT6
INT5
INT4
INT3
INT2
INT1
INT0
INTR 1/E0
INTA 1/E0
U23 LS148
VCC
GND
GS
EO
EI
U22 LS244
1EN
2EN
D3
D2
D1
D0
D4
D5
D6
D7

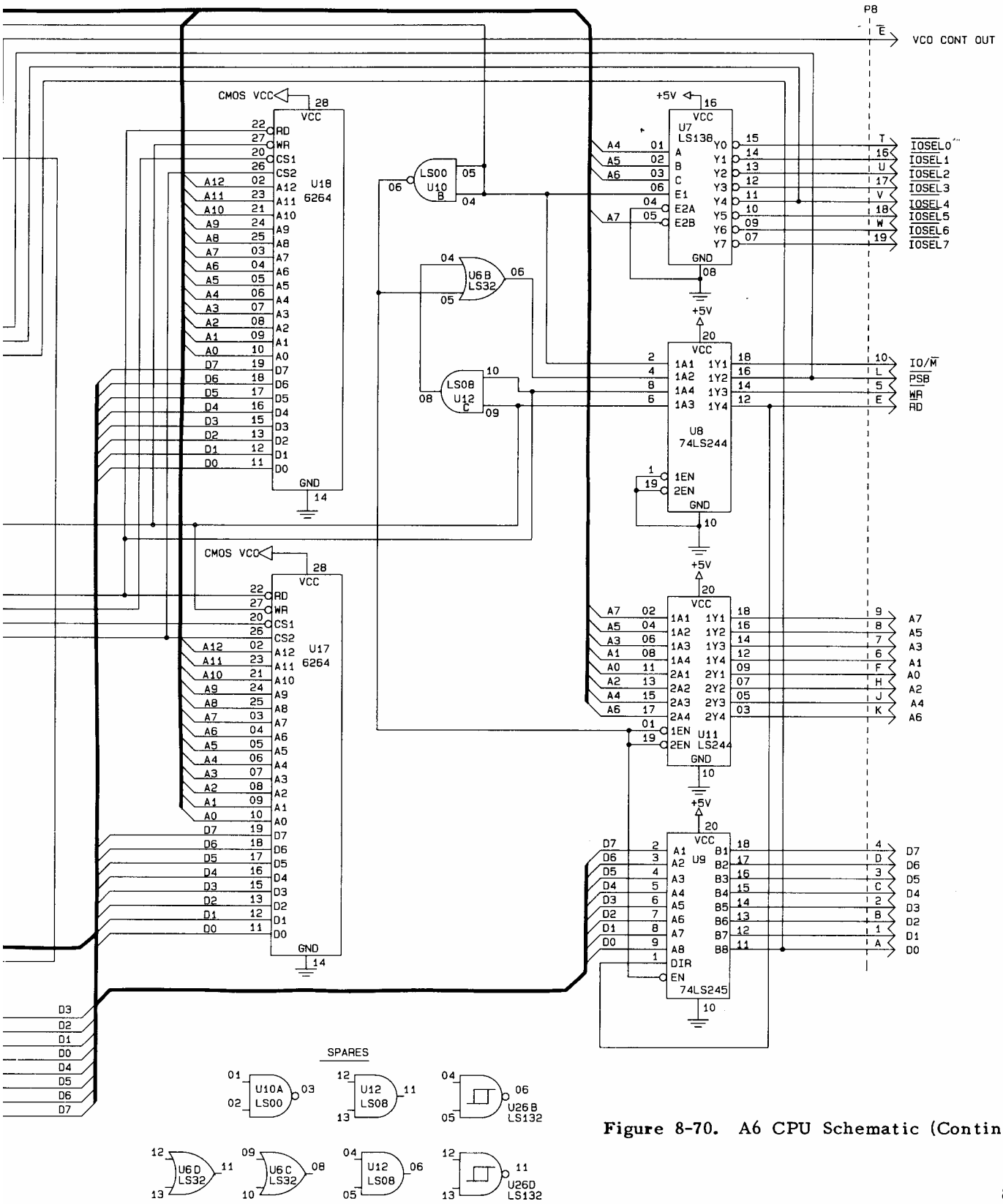


Figure 8-70. A6 CPU Schematic (Continued)

8-7.7 A7 Graphic Display Processor (GDP)

The GDP generates video timing, reading and writing from the three memory planes, memory refresh, and the continual process of reading out each line of information for display purposes.

The A7 block diagram is shown in Figure 8-80. The parts locator diagram and schematic are shown in Figures 8-81 and 8-82. Unless otherwise directed, refer to the block diagram (Figure 8-80) for the following circuit descriptions.

a. General. There are three memory planes on A7. Each plane is capable of providing 512 by 512 pixels (or other equivalent format). Since each memory plane needs to be 16-bits wide for the GDP, each memory plane consists of four memory chips, with each chip containing 16k x 4 of memory. The memory chips are comprised of U30 through U41.

All access to the A7 PCB and memory is through ports. The CPU (A6), however, cannot access the GDP memory directly.

The reading and writing process on A7 occurs only as instructed by the controlling microprocessor, U1.

The clock for the GDP is controlled by the phase-lock circuitry from A6. The clock is generated on A7 by a voltage tuned oscillator, with the video frame rate being returned to A6 for comparison and locking to the mains frequency. With this procedure, the display update is synchronized to ensure a stable display.

The video and timing signals are further processed to provide a composite video output (for external monitors), and a mixed video signal and timing signals for the 6400 CRT.

b. GDP Interface to A6. The U1 GDP IC performs all timing, update, and accesses to video memory functions necessary to form a graphic display. The CPU informs the GDP of types of graphic commands and coordinates. The GDP then carries out those commands.

The interface between A6 and A7 (Figure 6-71) is through two ports: one Write port for commands and one Write port for parameters. In order to examine the status of the GDP at any time, one of the ports can also be read. The port to be accessed is determined by A0. A0 is read if $\overline{RD}$ is LOW, and written to if $\overline{WR}$ is LOW. This information is mapped into the microprocessor's port map by U2, which gates the read and write lines with the port block--in this case, the port block is $\overline{IOSEL_6}$ which makes ports 60H to 6FH provide access to the GDP.

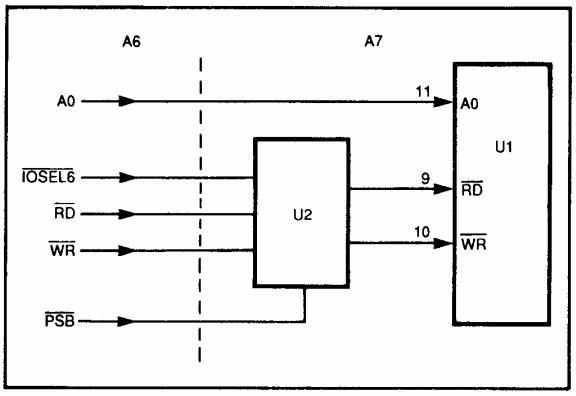


Figure 8-71. CPU Access to GDP

The other interface requirement is to the phase lock circuitry on A6. This circuitry compares the frame rate generated by the GDP with the line frequency (Figure 8-72), and provides a voltage to tune the clock for the GDP. This tuning voltage enters the board (Figure 8-73) through R40, the test jumper, and R38, C39, and L1 to the varicap, CR4. In the absence of a tuning signal, the test jumper enables the oscillator to run at approximately the correct frequency.

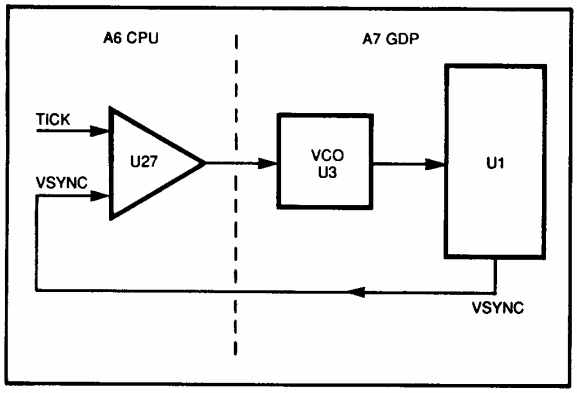


Figure 8-72. Phase-lock Loop Circuitry: A6 to A7

Those components preceding the varicap provide loop stability by filtering extraneous noise from the tuning signal. The clock signal is squared and buffered to the rest of the board by U43 and U3A. This signal is used to set the pixel clock. After dividing down, it also sets the main GDP clock (2 x W_{clk}).

c. GDP Interface to the CRT. The GDP produces the synchronization pulses HSYNC and VSYNC (Figure 8-74). These pulses are buffered (VSYNC is also inverted) by U8B and U13B before going to the CRT driver PCB.

Three planes of video are combined and mixed with a synchronized blanking signal (Figure 8-75). The blanking from U1 is synchronized to the actual clocking of the video data. This compensates for logic delays which could cause spurious display data to appear at the screen edges. This synchronization is performed by combining the blanking signal from U1 with the enable signal, which loads the video shift registers, at U6B. This combined signal is then gated with the three video signals by U13, and mixed at various video levels with R6 thru R11, CR1 thru CR3, and R22.

This mixed video is further amplified by Q1 and Q2, which is biased by R29 thru R30. The signal is then buffered by Q4 before going to the CRT section (edge connector pin 25). The signal is further mixed with composite synchronization signals through U4 to provide composite video by Q3, R31 thru R33, and C13, which goes to the edge connector pin $\overline{A}$. The ground is also taken to the surrounding edge connector pins.

Figure 8-76 shows the signal flow to the CRT via the monitor driver board. The CRT and its associated PCB are not field reparable.

d. Memory Access. All memory access is performed over the 16-bit bus AD0 thru AD15. Memory is read into U1, processed, and sent back over the same bus. This bus contains both data and address information.

Information flows from U1 (address information on AD0-AD15) to U15 (Figure 8-77), which latches in the high order addresses (AD8-AD15). The addresses are multiplexed by U16 and U17 to form the memory address bus MADR0-MADR7. Resistors R12, R2, R3, R13, R5, R14, R38, and R39 prevent this high speed, multiplexed, address bus from ringing.

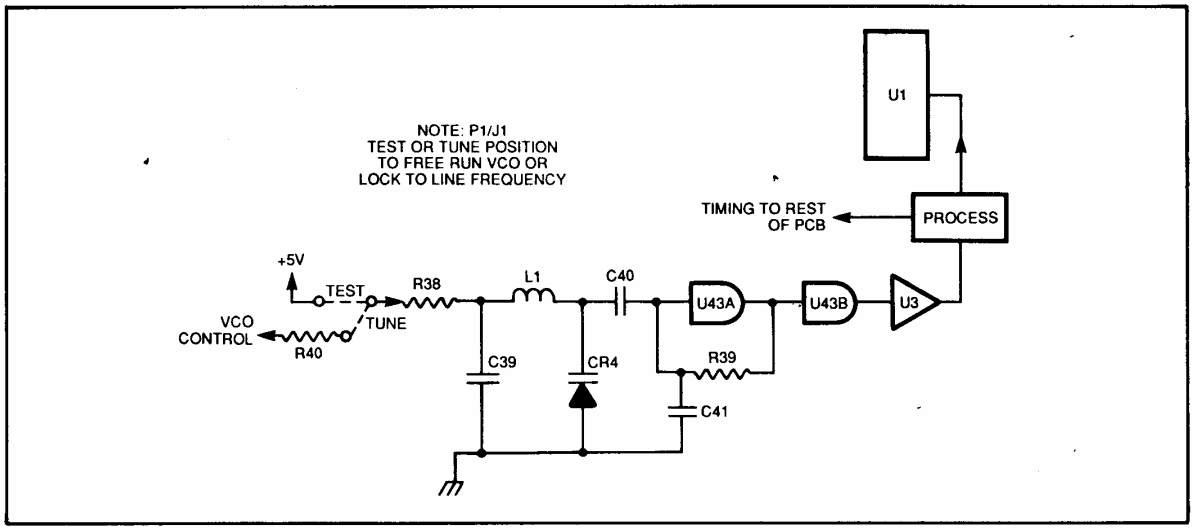


Figure 8-73. Phase-lock Loop Circuitry

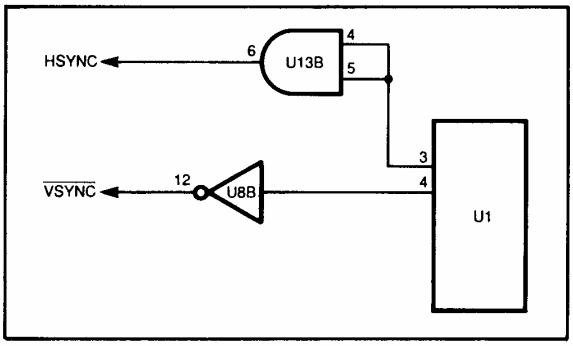


Figure 8-74. GDP Syncronization Pulses

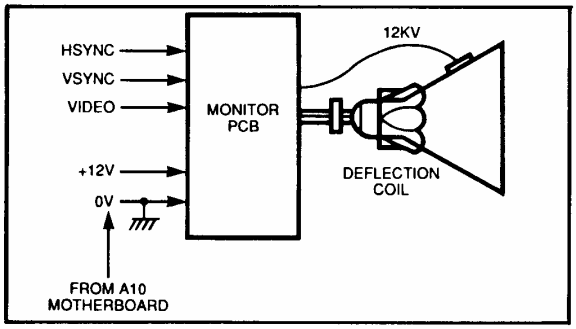


Figure 8-76. CRT Driver Board

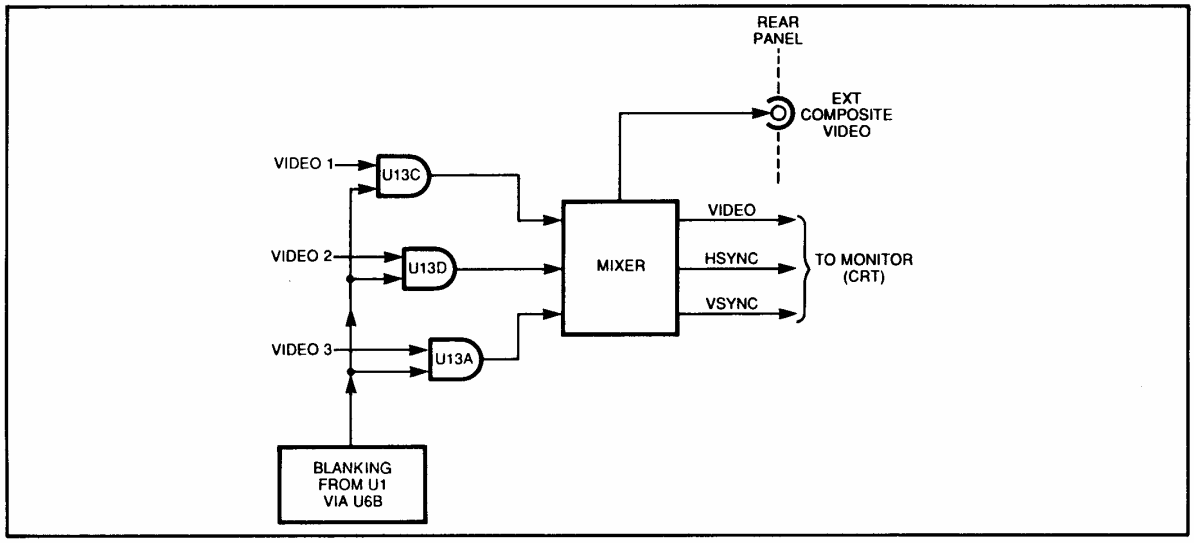


Figure 8-75. GDP Interface to Monitor

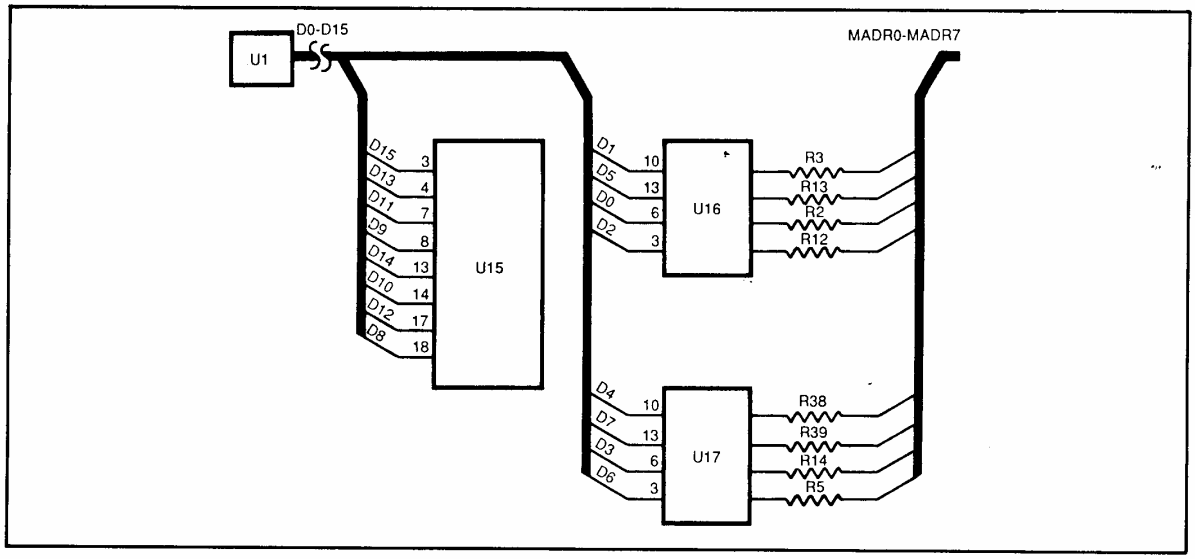


Figure 8-77. Formation of Memory Address Bus

Timing for the latching of U15 and the switching of U16 and U17 is generated in the timing section (paragraph 8-7.7e). The whole address is latched into the memory chips (U30-U33 for plane 0) using the Row Address Strobe ($\overline{RAS}$) (pin 5 on each memory IC) and Column Address Strobe ($\overline{CAS}$) (pin 16 on each memory IC) both of which are generated by the timing logic.

The data of the memory location addressess, if in a READ cycle, is presented to the internal bus VDO0-VDO15 when the IC is enabled by the output enable (OE) control line (pin 1 on all memory ICs). If in a WRITE cycle, as in the update of display memory, the GDP chip (U1) ensures that data is available on these lines that pass through U20 and U21. For display cycles, the data is clocked into the shift registers U18 and U19 by the LOAD signal, LD (pin 15 of U18 and U19). Video memory planes 1 and 2 operate similarly.

Memory plane 1 contains the A channel trace and trace identifier; plane 2 contains the B channel trace and trace identifier; and plane 0 contains all other information including graticule, markers, and alphanumerics. The memory timing signals are shown in Table 8-13.

e. Logic Timing. Timing sequences (Figure 8-78) are provided by a sequence generator formed by U5 and U9. U5 counts the pixel clock from U3A, pin 2. U9 takes the address latch enable line $\overline{ALE}$ (U1, pin 6, inverted by U8D) as a serial input, and clocks the signal through the IC at pixel rate so that $\overline{ALE}$ is at the phase shifted outputs of QA and QC (pins 15 and 13).

Timing signals $\overline{RAS}$, $\overline{CAS}$, and the multiplexer select signal, $\overline{ROW\text{-}ADR\text{-}SEL}$, are generated by gating $\overline{ALE}$ and the phase shifted $\overline{ALE}$ with U10. The $\overline{RAS}$ and $\overline{CAS}$ signals are then driven by U42B through the anti-ringing resistors R17 and R18 to the memory ICs. The $\overline{OE}$ signal is derived in a similar way using U11.

To access the three memory planes, the A16 and A17 address lines from U1 (pins 38 and 39) must be decoded.

Table 13. Memory Timing Signals

Signal	Location	Action
CK	U18-U19, pin 7	Clocks out data at pixel rate.
$\overline{LD}$	U18-U19, pin 15	Loads 16 bits to shift reg (U18, U19)
Qh	U19, pin 13	Video (plane 0) data out
DIR	U20-U21, pin 1	Determines read or write from/to memory ICs U30-U33.
$\overline{EN}$	U20-U21, pin 19	Controls tri-state of buffers, prevents data conflict.
$\overline{WE}$	U30-U33, pin 4	Low allows data write to memory.
$\overline{RAS}$	U30-U33, pin 5	Latches in part of address.
$\overline{CAS}$	U30-U33, pin 16	Latches in other part of address.
$\overline{OE}$	U30-U33, pin 1	Controls output of memory to bus VDO0-VDO15. Prevents conflict.

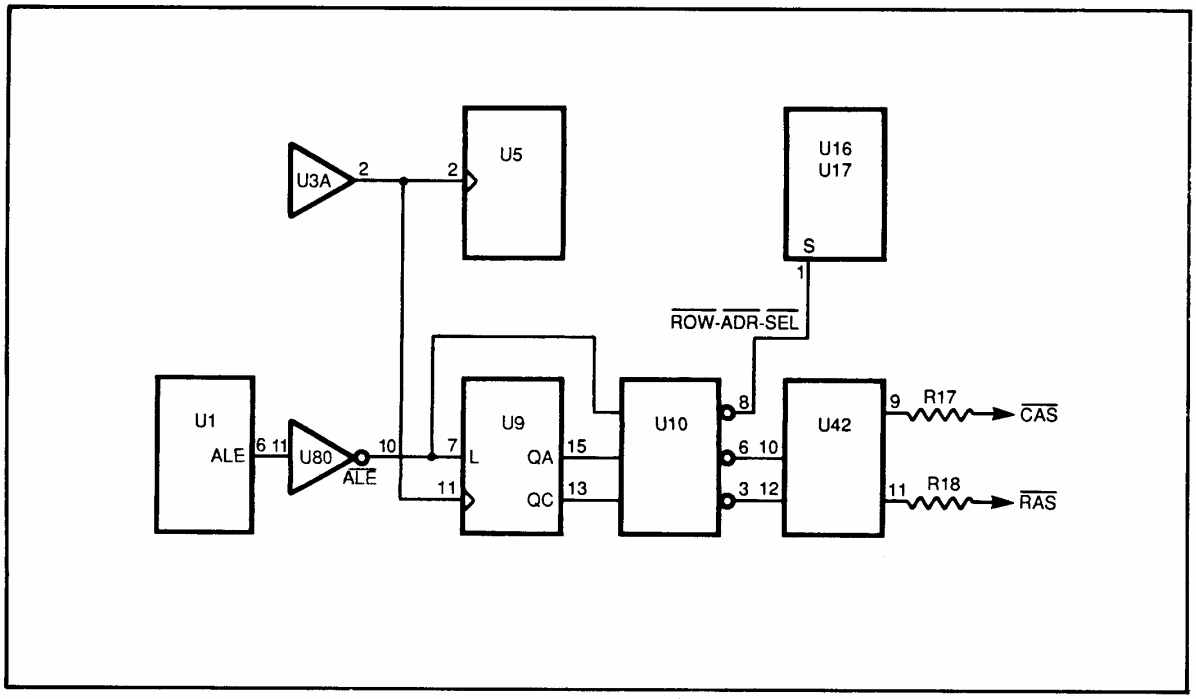


Figure 8-78. Logic Timing

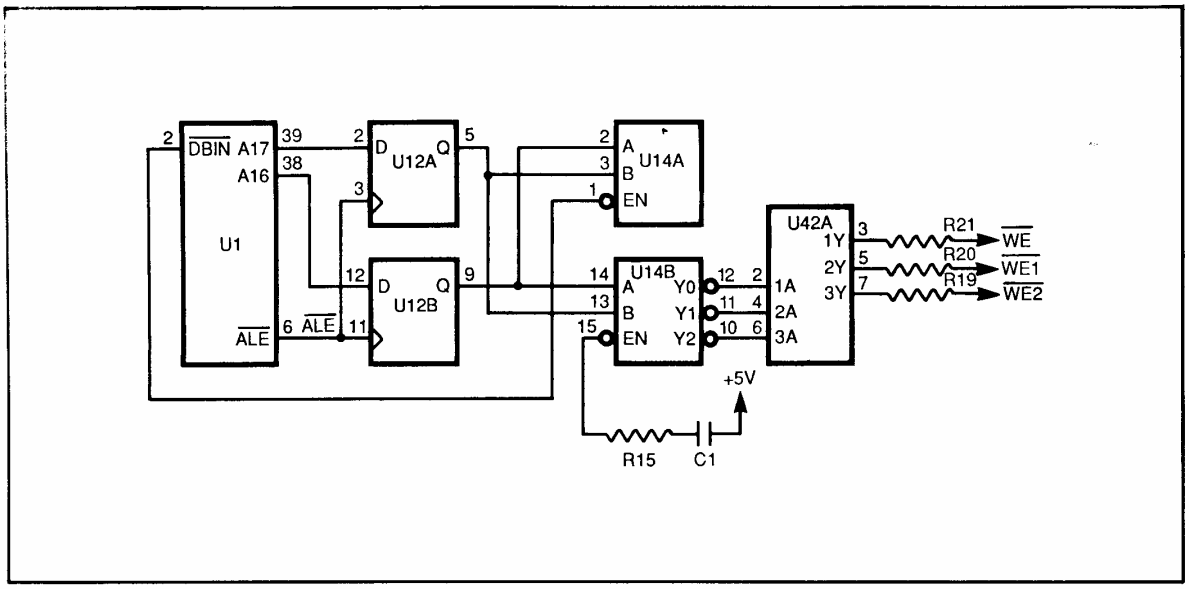
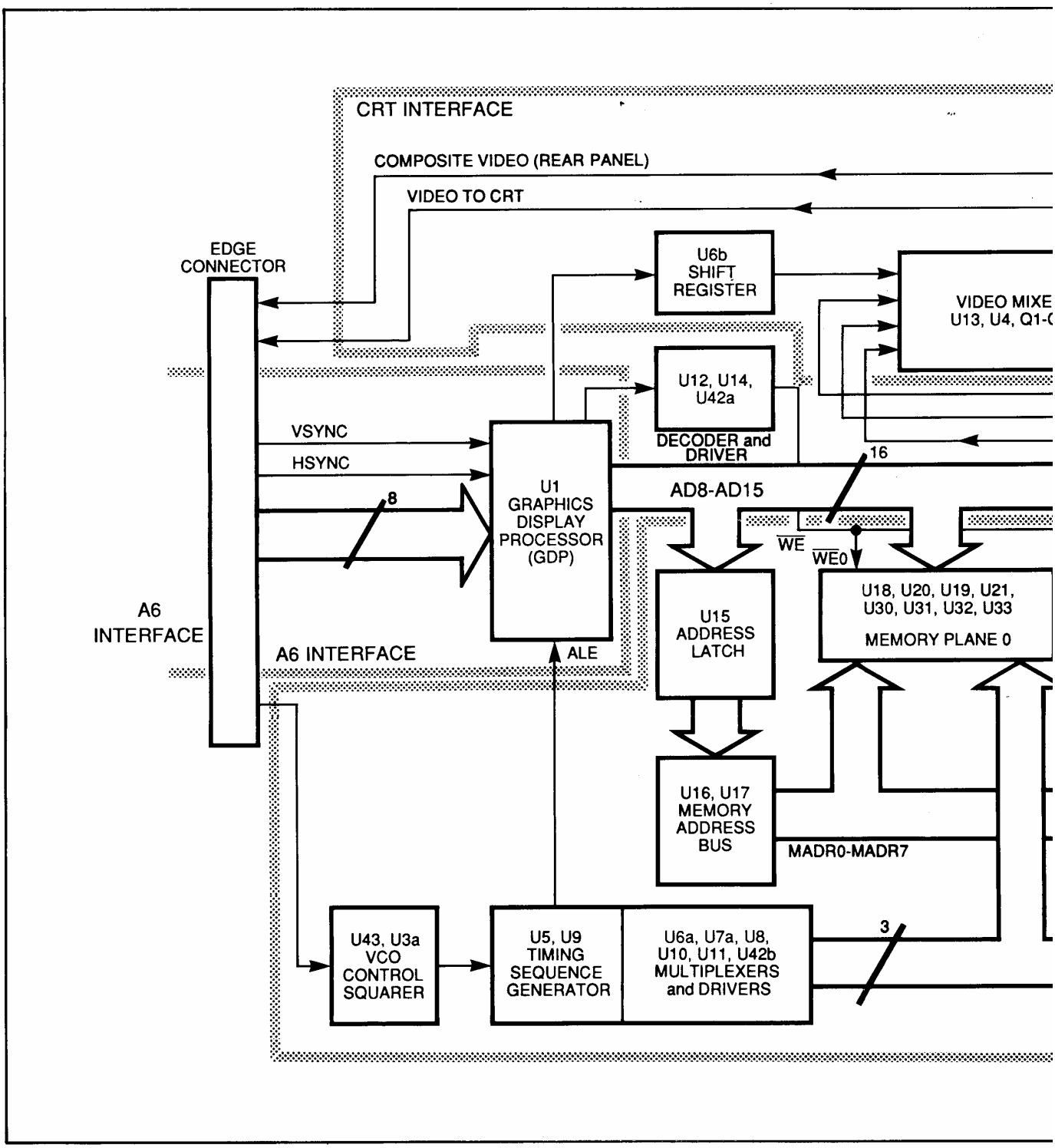


Figure 8-79. Decoding Address Lines and Enable Lines

Since these lines are not valid at all times, they are latched by U12 (Figure 8-79), along with the conrol line $\overline{ALE}$ from U1. These decoded lines provide four lines (only three of which are used) corresponding to each of the four blocks of memory covered by A16 and A17.

By further gating these signals with the $\overline{DBIN}$ (U1, pin 2) signal, separate enable signals can be provided for the bi-directional bus drivers, U20 and 21 ($\overline{WE}$v$\overline{DBIN}$) of the video memory planes. Similarly, the $\overline{WE}$ lines are also derived for the memory ICs; in this case it is necessary to introduce a small delay using R15 and C1 to allow for the turn-around time of the bi-directional buffers.

This delay action ensures that the buffers have turned around to drive data to the memories and that the data has settled before the Write Enable line is pulsed on the memories. The separate $\overline{WE}$ lines are driven by U42A through anti-ringing resistors R19 thru R21.


CRT INTERFACE
COMPOSITE VIDEO (REAR PANEL)
VIDEO TO CRT
EDGE CONNECTOR
U6b SHIFT REGISTER
VIDEO MIXE
U13, U4, Q1-
U12, U14, U42a
DECODER and DRIVER
VSYNC
HSYNC
8
16
U1 GRAPHICS DISPLAY PROCESSOR (GDP)
AD8-AD15
WE
WE0
U15 ADDRESS LATCH
U18, U20, U19, U21, U30, U31, U32, U33
MEMORY PLANE 0
A6 INTERFACE
A6 INTERFACE
ALE
U16, U17 MEMORY ADDRESS BUS
MADR0-MADR7
U43, U3a VCO CONTROL SQUARER
U5, U9 TIMING SEQUENCE GENERATOR
U6a, U7a, U8, U10, U11, U42b MULTIPLEXERS and DRIVERS
3

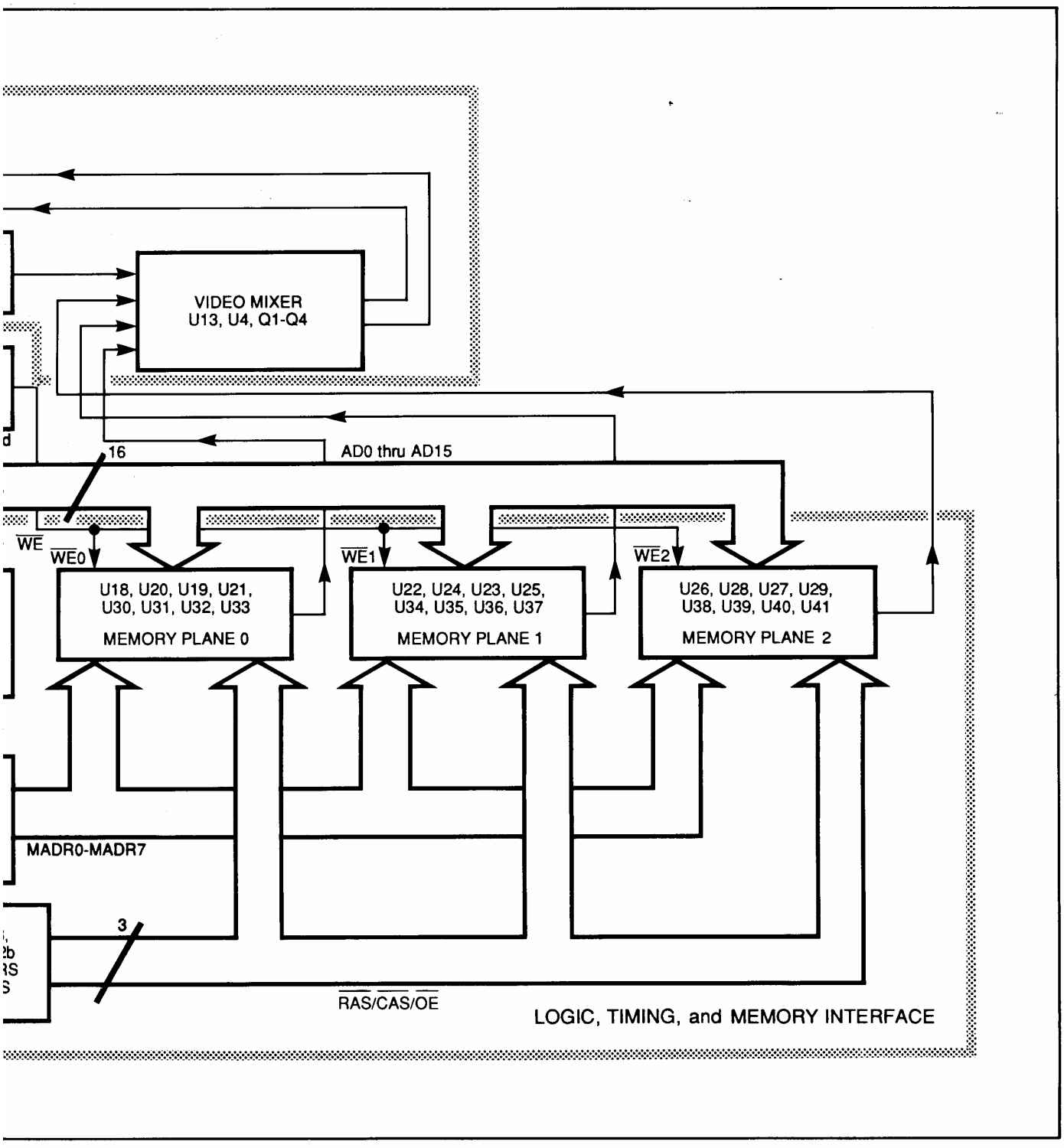


Figure 8-80. A7 GDP Block Diagram

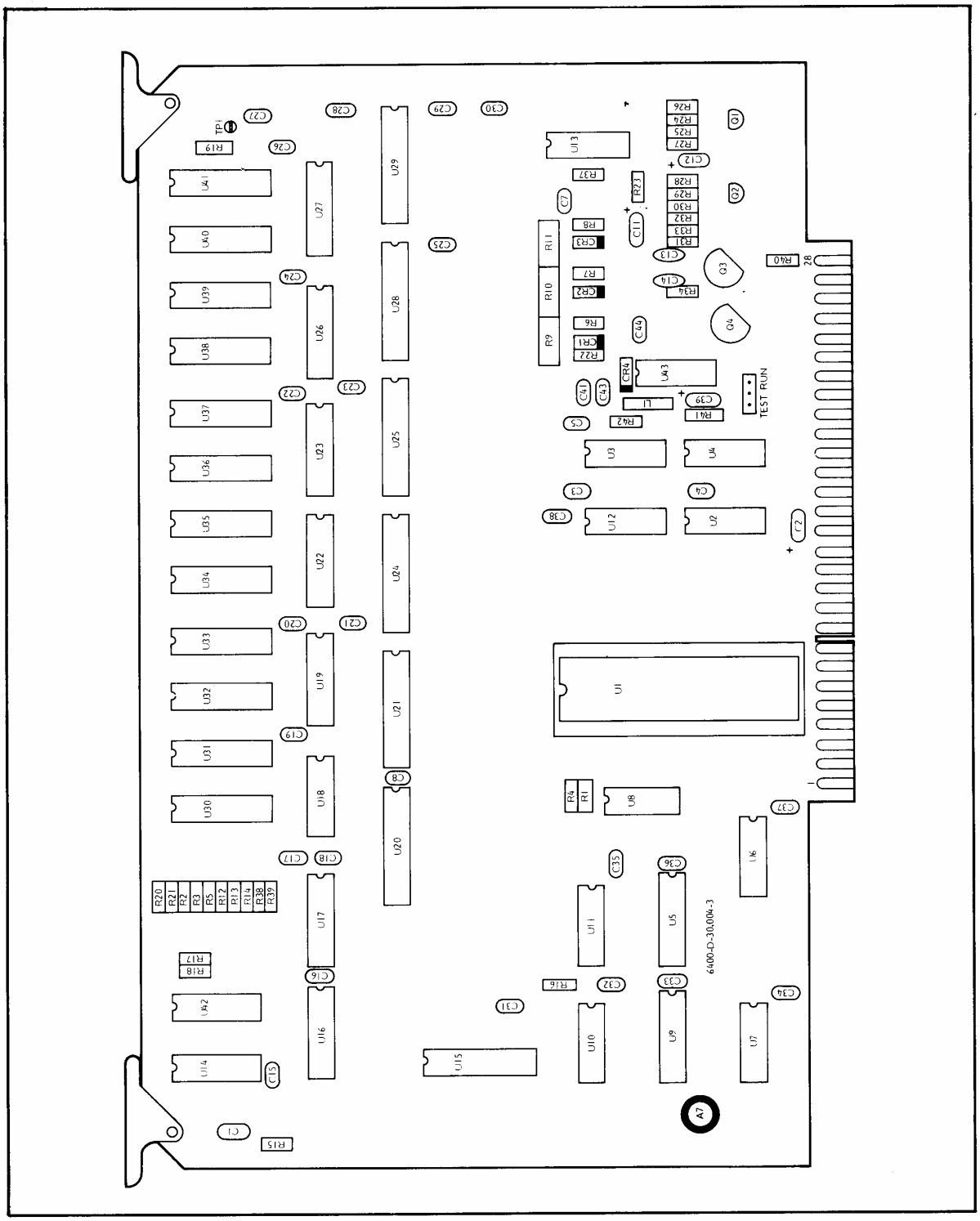
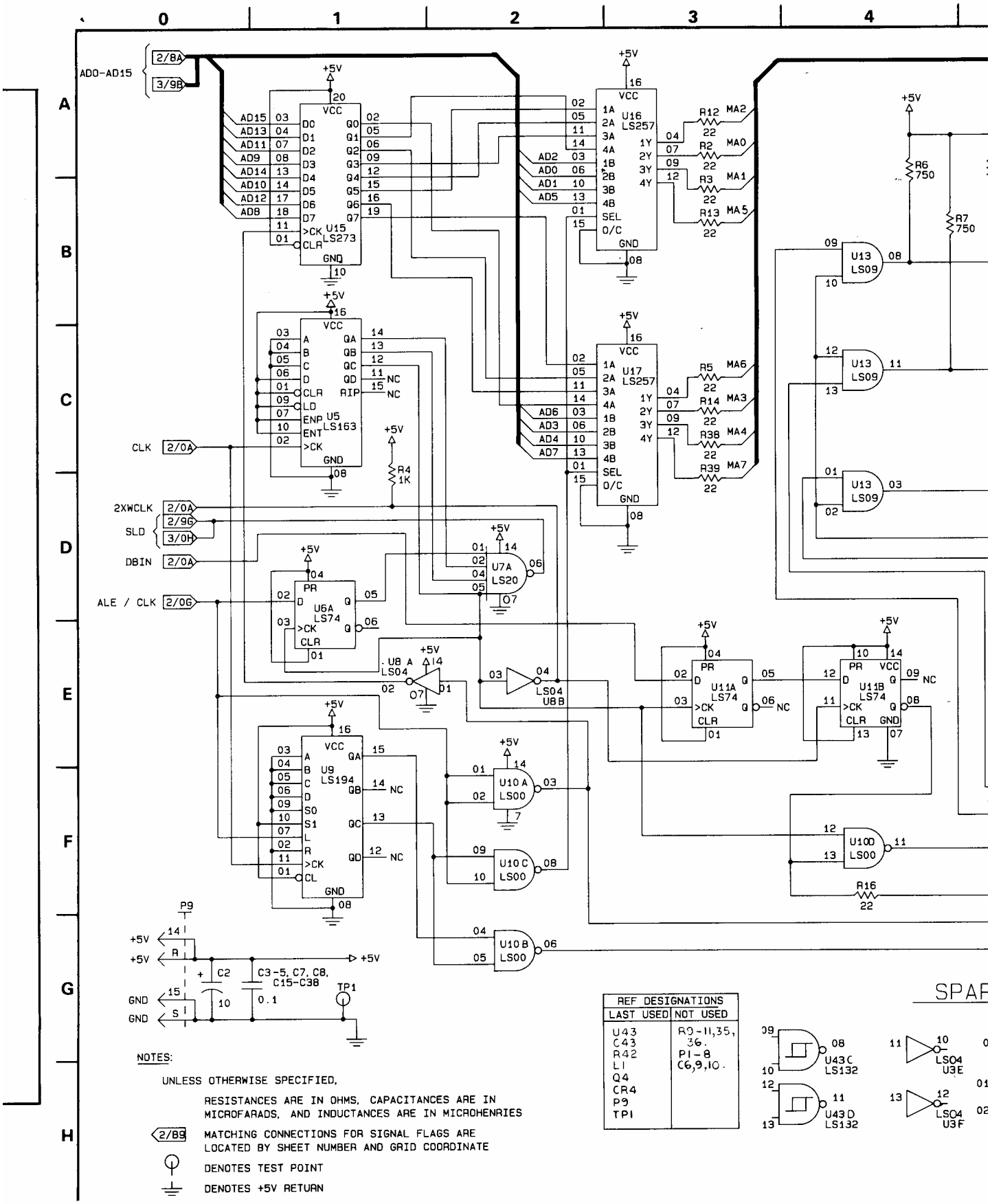
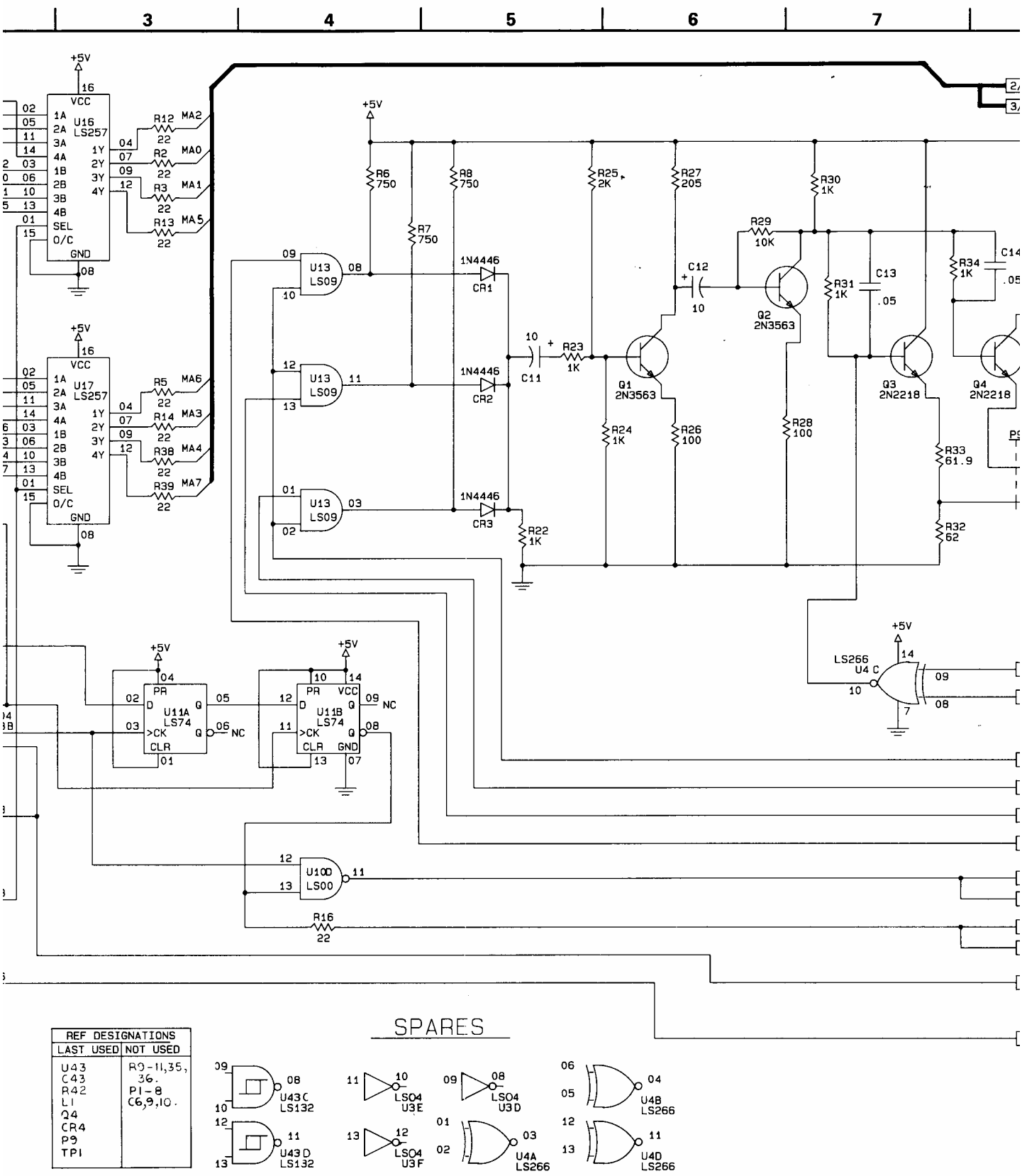


Figure 8-81. A7 PCB Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
AD0-AD15
2/8A
3/9B
U15 LS273
U16 LS257
U17 LS257
U5 LS163
U6A LS74
U7A LS20
U8 A LS04
U8 B LS04
U9 LS194
U10 A LS00
U10 B LS00
U10 C LS00
U10D LS00
U11A LS74
U11B LS74
U13 LS09
U43C LS132
U43D LS132
U3E LS04
U3F LS04
CLK
2XWCLK
SLD
DBIN
ALE / CLK
R2 22
R3 22
R4 1K
R5 22
R6 750
R7 750
R12 22
R13 22
R14 22
R16 22
R38 22
R39 22
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
P9
C2 10
C3-5, C7, C8, C15-C38 0.1
TP1
REF DESIGNATIONS
LAST USED
NOT USED
U43
C43
R42
L1
Q4
CR4
P9
TP1
R9-11,35, 36.
P1-8
C6,9,10.
NOTES:
UNLESS OTHERWISE SPECIFIED,
RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS, AND INDUCTANCES ARE IN MICROHENRIES
2/8B MATCHING CONNECTIONS FOR SIGNAL FLAGS ARE LOCATED BY SHEET NUMBER AND GRID COORDINATE
DENOTES TEST POINT
DENOTES +5V RETURN
SPAR



REF DESIGNATIONS	
LAST USED	NOT USED
U43 C43 R42 L1 Q4 CR4 P9 TP1	R9-11,35, 36. P1-8 C6,9,10.

SPARES

U43C LS132
U43D LS132
U3E LS04
U3D LS04
U3F LS04
U4A LS266
U4B LS266
U4D LS266

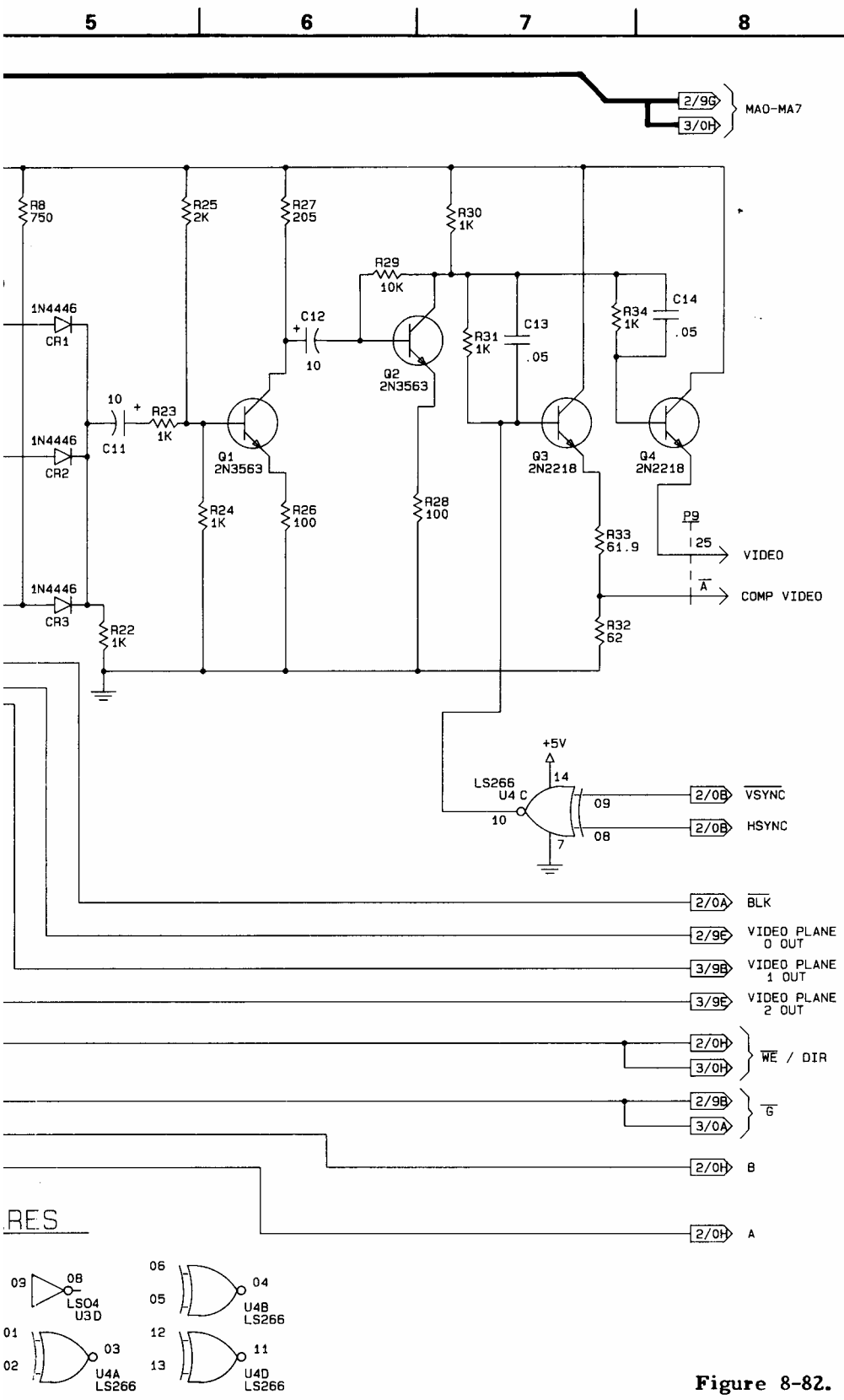
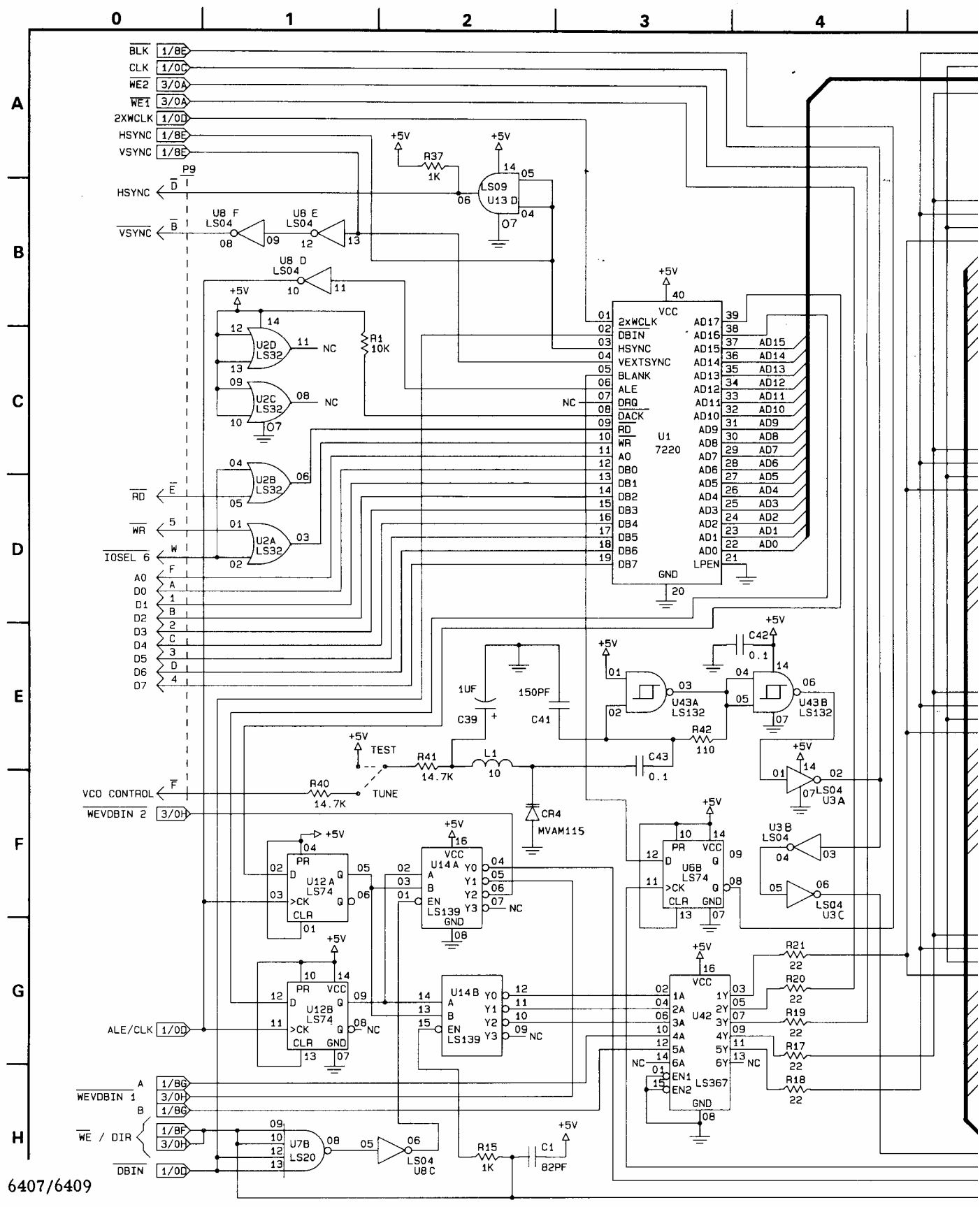


Figure 8-82. A7 GDP Schematic


0
1
2
3
4
A
B
C
D
E
F
G
H
BLK 1/8E
CLK 1/0C
WE2 3/0A
WE1 3/0A
2XWCLK 1/0D
HSYNC 1/8E
VSYNC 1/8E
HSYNC
VSYNC
RD
WR
IOSEL 6
A0
D0
D1
D2
D3
D4
D5
D6
D7
VCO CONTROL
WEVDBIN 2
ALE/CLK 1/0D
WEVDBIN 1 3/0H
WE / DIR 1/8F 3/0H
DBIN 1/0D
U8 F LS04
U8 E LS04
U8 D LS04
R37 1K
LS09 U13 D
U2D LS32
U2C LS32
U2B LS32
U2A LS32
R1 10K
NC
U1 7220
2xWCLK
DBIN
HSYNC
VEXTSYNC
BLANK
ALE
DRQ
DACK
RD
WR
A0
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
LPEN
VCC
GND
+5V
1UF C39
150PF C41
C42 0.1
C43 0.1
R42 110
R41 14.7K
L1 10
R40 14.7K
TEST
TUNE
CR4 MVAM115
U43A LS132
U43B LS132
U3A LS04
U3B LS04
U3C LS04
U12A LS74
U12B LS74
U6B LS74
U14A LS139
U14B LS139
U42 LS367
R21 22
R20 22
R19 22
R17 22
R18 22
U7B LS20
U8C LS04
R15 1K
C1 82PF

6407/6409

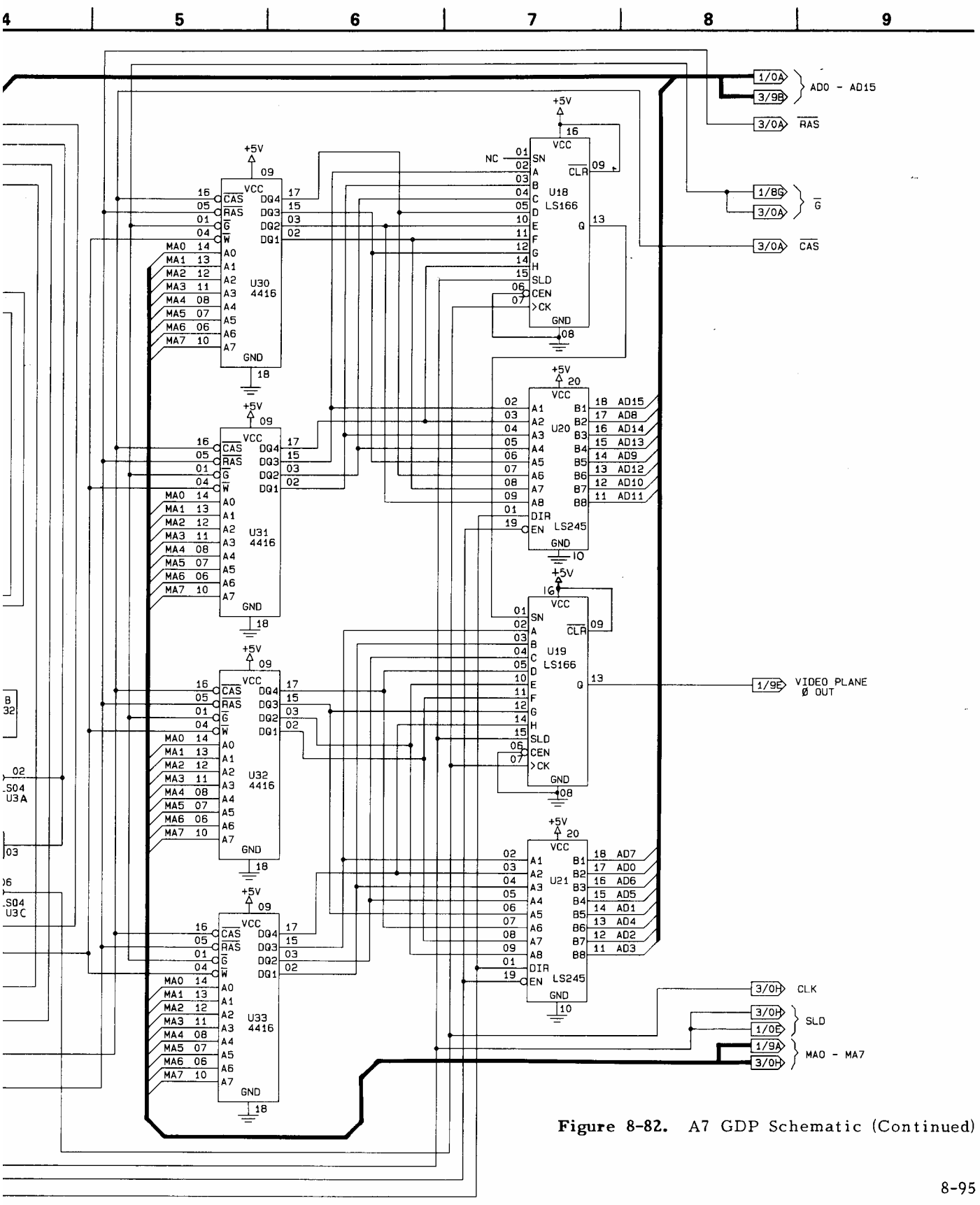
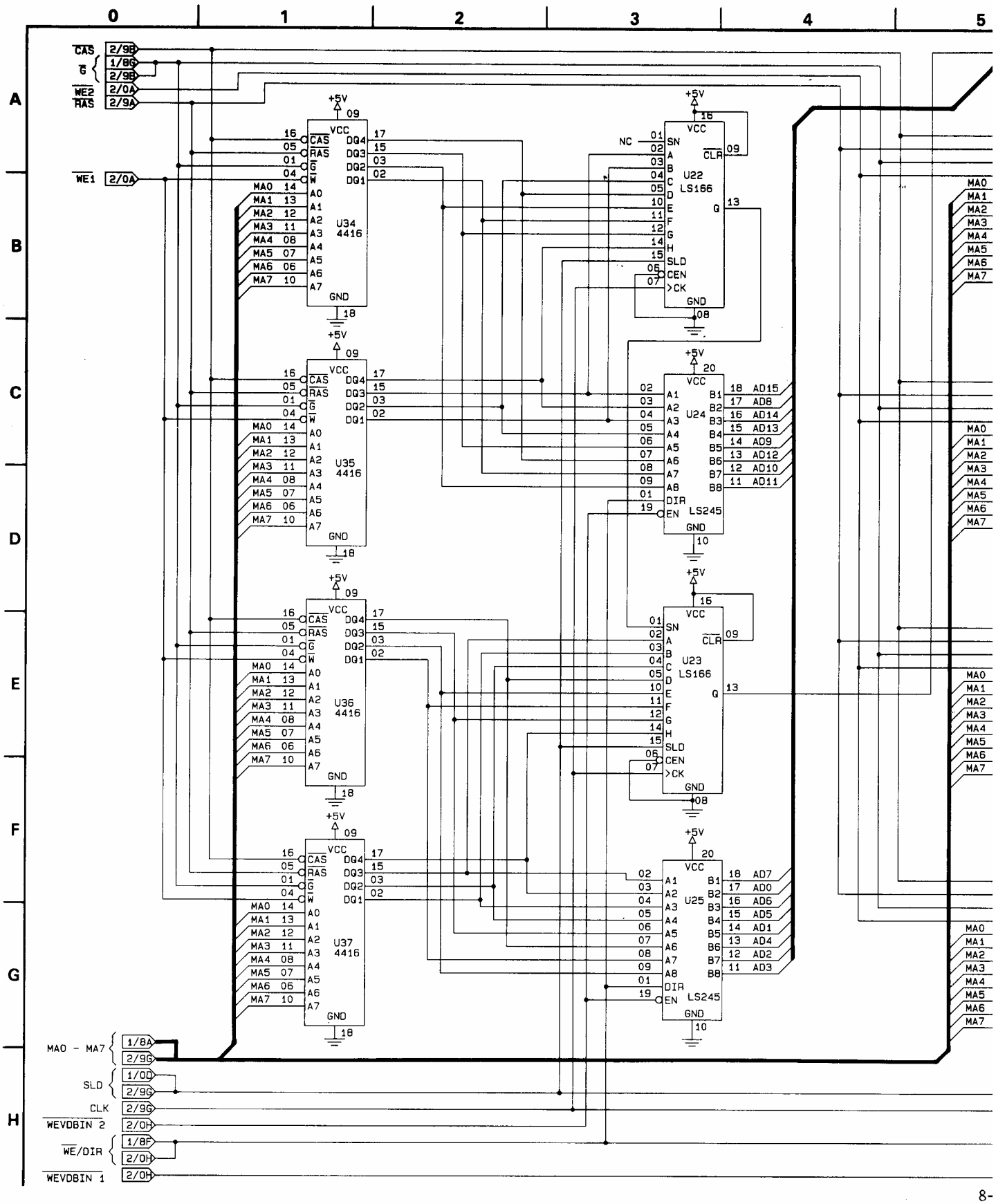


Figure 8-82. A7 GDP Schematic (Continued)


0
1
2
3
4
5
A
B
C
D
E
F
G
H
CAS
G
WE2
RAS
WE1
MA0 - MA7
SLD
CLK
WEVDBIN 2
WE/DIR
WEVDBIN 1
+5V
VCC
GND
U34 4416
U35 4416
U36 4416
U37 4416
U22 LS166
U23 LS166
U24 LS245
U25 LS245
NC
SN
CLR
SLD
CEN
>CK
DIR
EN
AD15
AD8
AD14
AD13
AD9
AD12
AD10
AD11
AD7
AD0
AD6
AD5
AD1
AD4
AD2
AD3

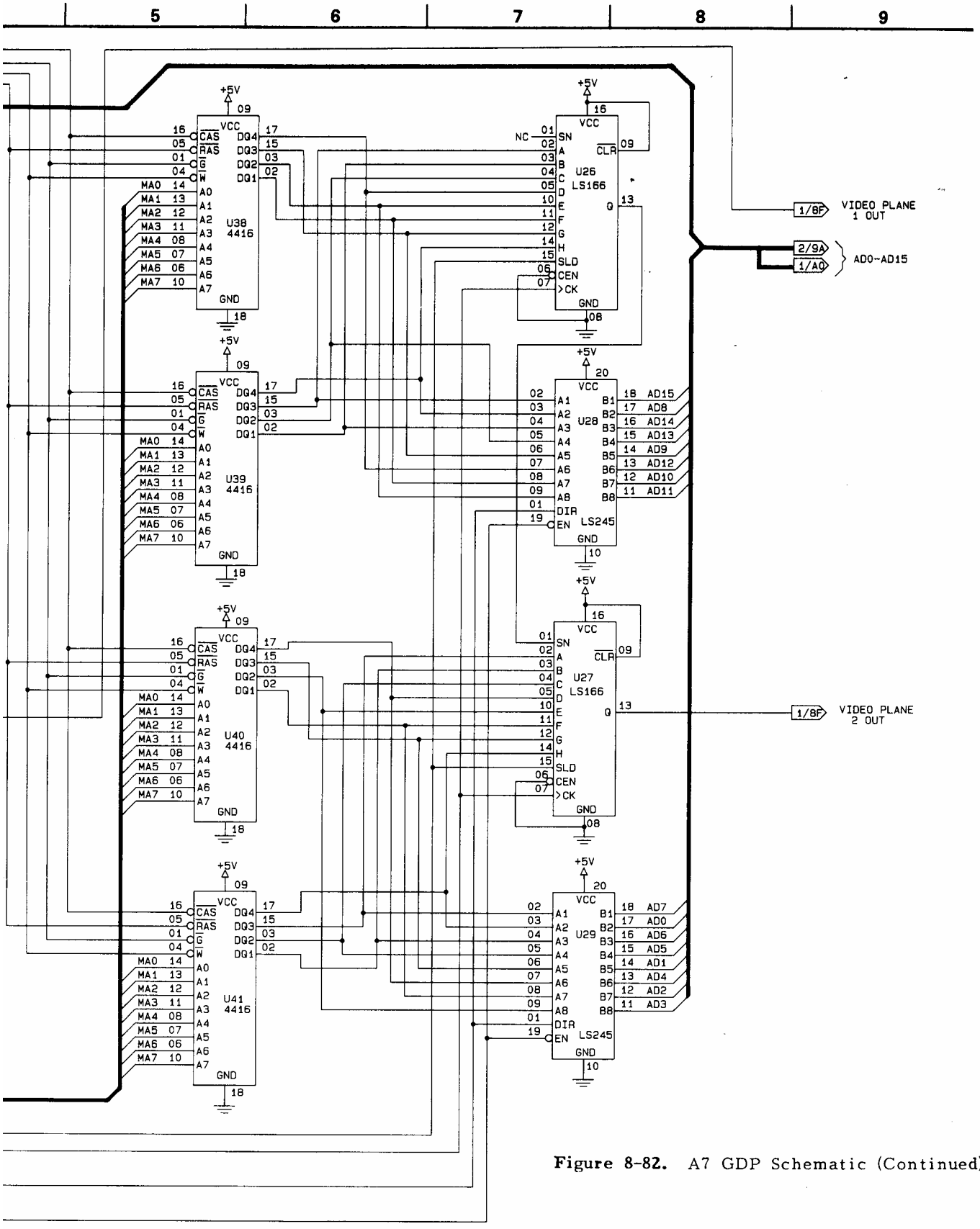


Figure 8-82. A7 GDP Schematic (Continued)

8-7.8 A8 GPIB Option

The A8 PCB interfaces the 6400 to the General Purpose Interface Bus (GPIB). The circuit block diagram is shown in Figure 8-84. The parts locator diagram and schematic are shown in Figures 8-85 and 8-86. Refer to the block diagram for the following discussion.

a. General. The GPIB option fits into a slot on the back of the rear panel and plugs into the mother board with a twenty-way ribbon cable/connector, that carries both data and power.

b. Protocol and Timing. GPIB protocols and timings are handled through controller chip U1, which occupies the I/O ports 050H thru 057H. Signals are buffered to and from the IEEE-488 P2 interface connector by Bus Transceivers U2, U3, U4, and U5. These transceivers transmit and receive the GPIB data while protecting U1 from damage external to A8. With no power applied, these transceivers will not affect or be affected by the GPIB Bus. What this protection means is that the 6400 can remain connected to an active bus, and even if the 6400 is not turned on it will not cause or receive any damage.

c. Bus Address. The 6400's bus address is set using rear panel DIP switch S1. When the 6400 is first turned on, the switch address value is read by the system through data latch U9 (Figure 8-83). Latch U9 is enabled when address lines A0 thru A3 are all logic HIGH (I/O port 05FH) and when $\overline{IOSEL_5}$ and $\overline{RD}$ are logic LOW. The A0-A3 address lines are decoded via gates U7B, U7C, U7D, U8C, U6B and U6C. Gate U6A decodes the chip select ($\overline{CS}$) for U1. Address line A3 is ANDed with $\overline{IOSEL_5}$ to set the $\overline{CS}$ line and map the controller into the port space 050H to 057H.

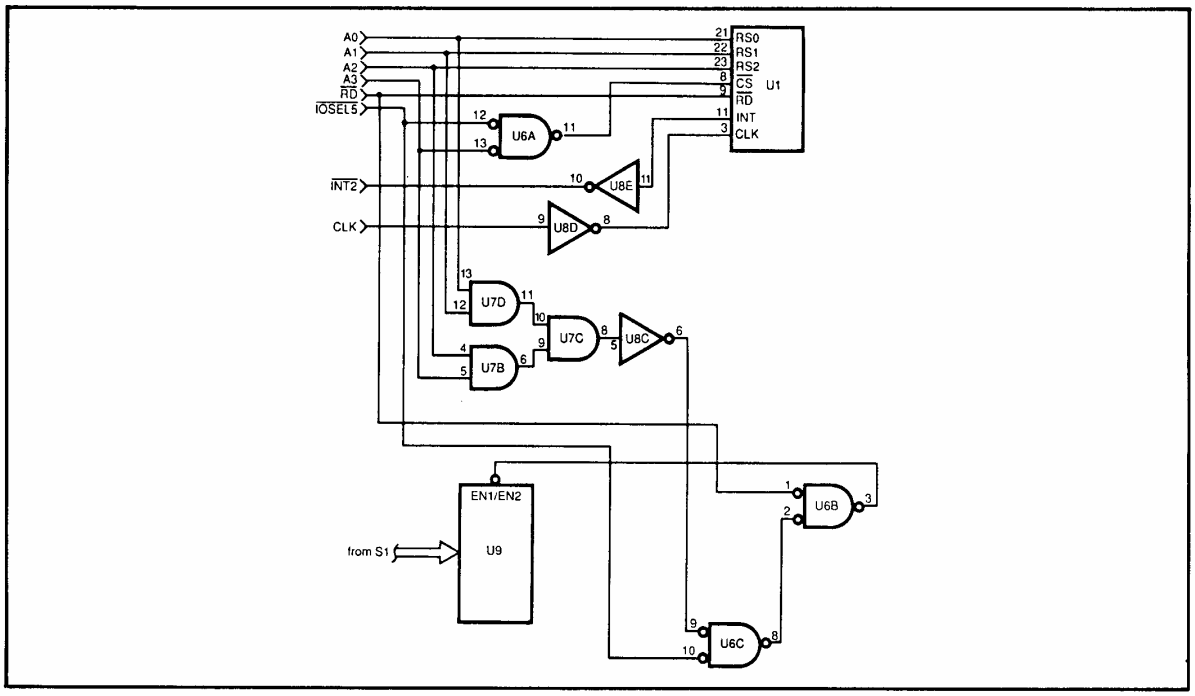


Figure 8-83. Bus Address Circuitry

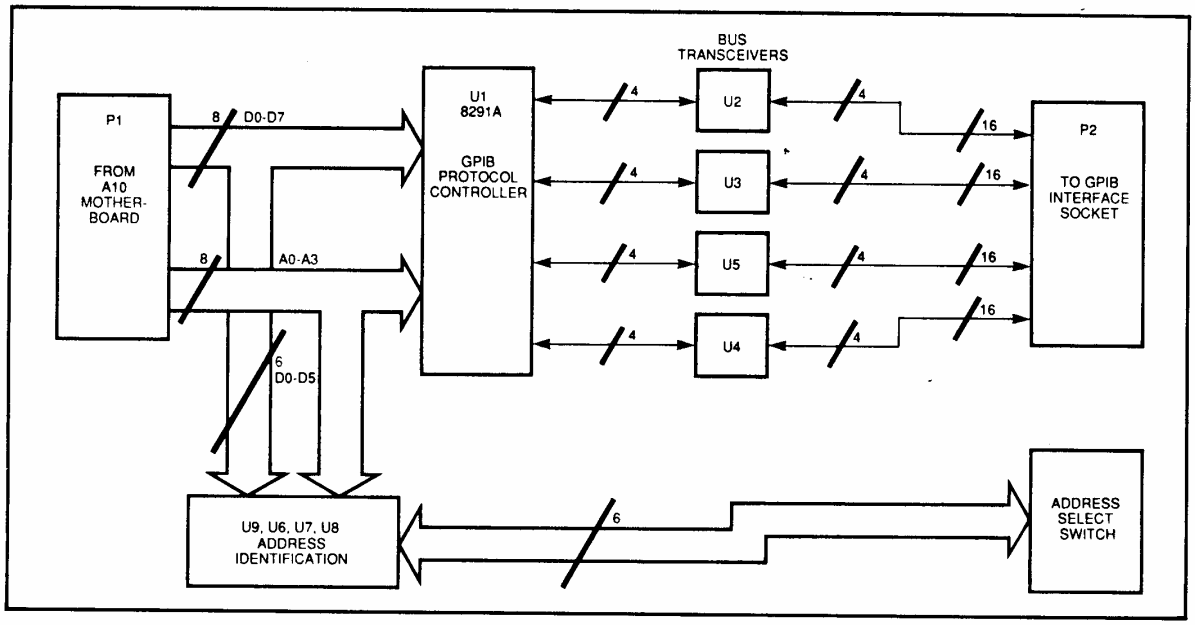


Figure 8-84. A8 GPIP Block Diagram

The 6400 bus address, which has been set using switch S1, is read when the instrument is turned on. If the address is changed while the instrument is operating, the RETURN TO LOCAL button must be pressed to allow the new address to be loaded.

d. Buffering. The remaining sections of U8 perform buffering functions:
   1. U8E buffers and inverts the interrupt output of U1 to drive the $\overline{INT_2}$ line.
   2. U8D buffers the incoming clock signal.

Since the transmit/receive control line from controller U1 is used by more than one TTL load, the signal is buffered, and inverted where necessary, by U8A and B.

e. Interrupts. Once U1 has been initialized it needs no regular attention. If a bus transaction takes place that concerns the 6400, U1 exerts an $\overline{INT_2}$ interrupt. The CPU then responds by interrogating U1 to establish the cause of the interrupt before taking appropriate action.

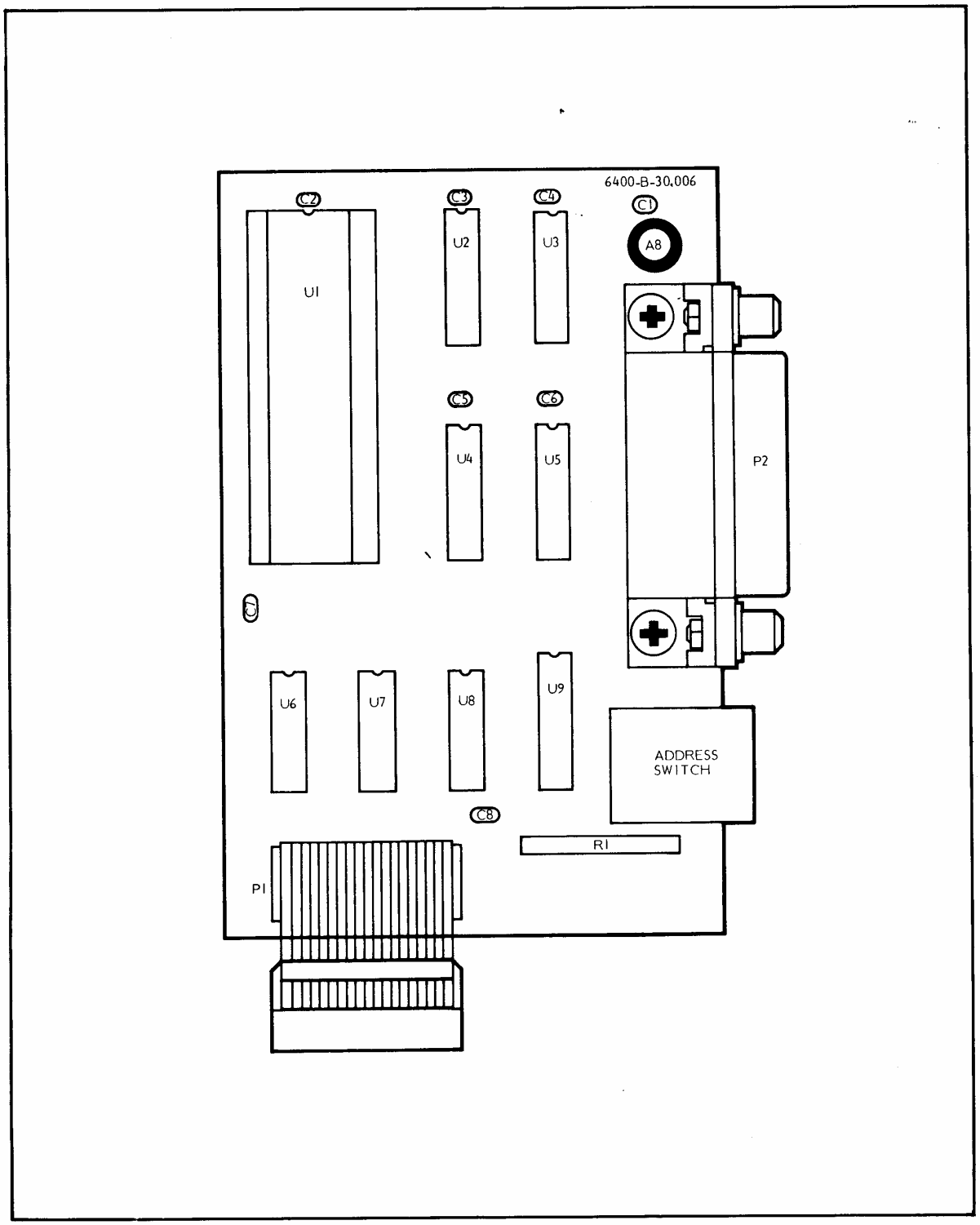
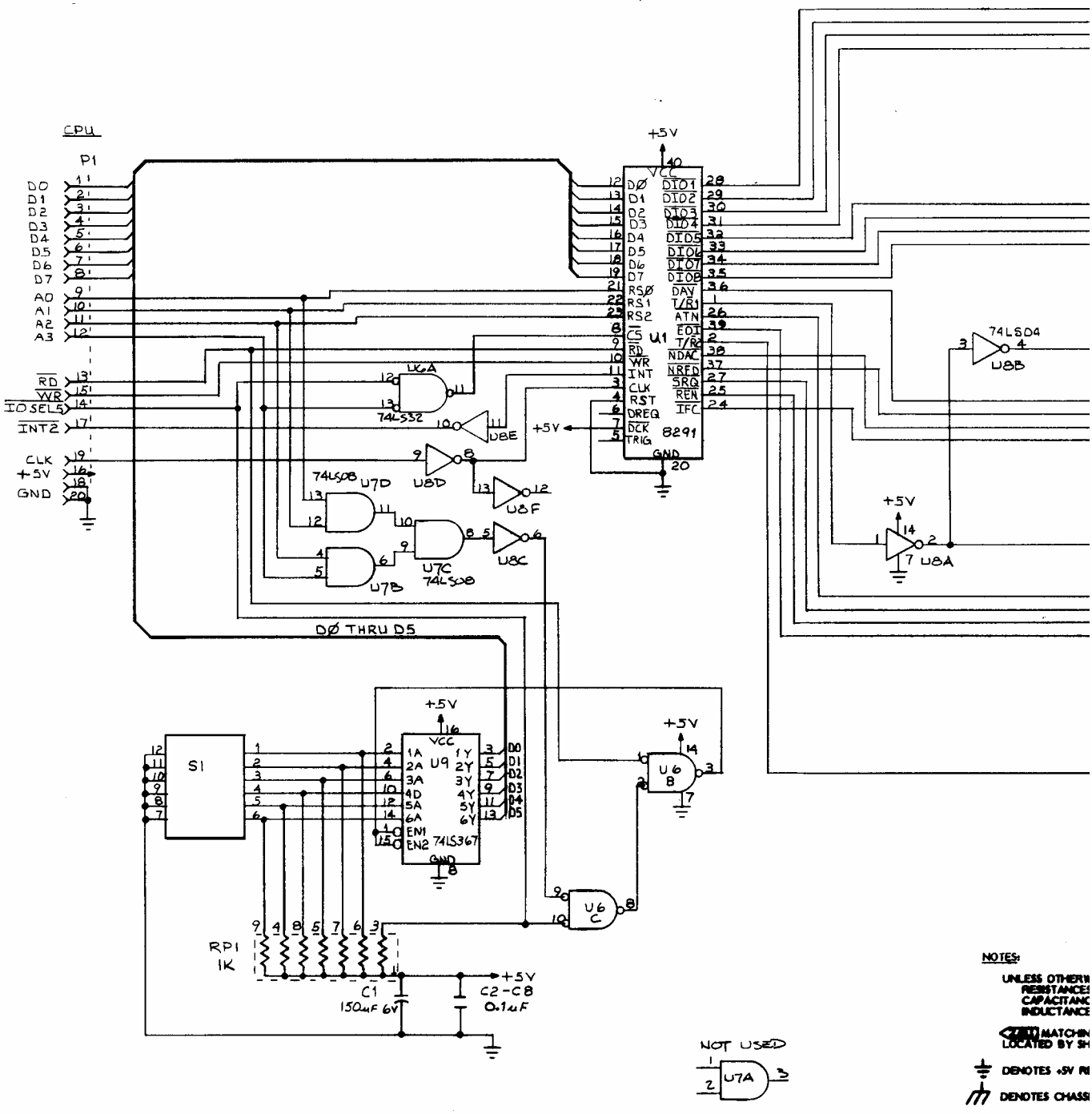
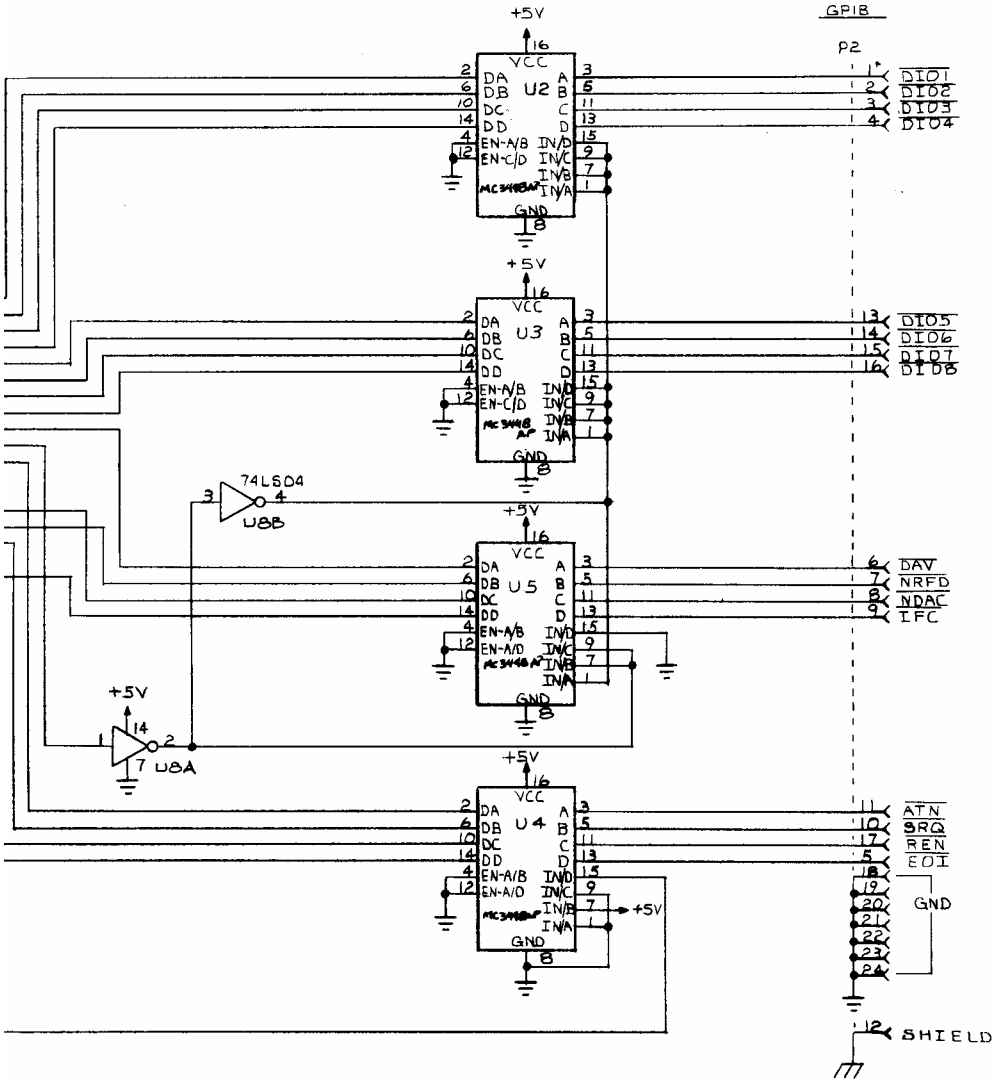


Figure 8-85. A8 PCB Parts Locator Diagram


CPU
P1
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
RD
WR
IOSEL5
INT2
CLK
+5V
GND
D0 THRU D5
U1
8291
U4A
74LS32
U8E
U8D
U8F
U8C
U7C
74LS08
U7D
U7B
74LS04
U8B
U8A
+5V
S1
U9
74LS367
U6B
U6C
RP1
1K
C1
150uF 6V
C2-C8
0.1uF
NOT USED
U7A
NOTES:



NOTES:

UNLESS OTHERWISE SPECIFIED,
RESISTANCES ARE IN OHMS.
CAPACITANCES ARE IN MICROFARADS.
INDUCTANCES ARE IN MICROHENRIES.

MATCHING CONNECTIONS FOR SIGNAL FLAGS ARE LOCATED BY SHEET NUMBER AND GRID COORDINATE.

DENOTES +5V RETURN.

DENOTES CHASSIS GROUND.

Figure 8-86. A8 GPIB Schematic

8-7.9 A9 Power Supply PCB

The A9 PCB provides eight regulated voltages. These voltages are shown in Table 8-14. The block diagram, parts locator diagram, and schematic are shown in Figures 8-88, 8-89, and 8-90 respectively.

a. General. The input to the A9 PCB is provided by the line voltage selector module on the rear panel. This module contains a line fuse and a line filter, and allows the use of either of four international line voltages: 100, 120, 220, and 240 Vac.

Two cable harnesses come from the input module, one goes to the front panel mounted line ON/OFF switch, and the other goes to the toroidal transformer mounted on the A10 motherboard. Another cable harness takes the secondary ac voltages from the transformer to input connector P3 of the A9 power supply PCB as shown on the schematic (Figure 8-90).

The power supply is a multi-rail, linear unit that provides the outputs shown in Table 8-14.

The regulated outputs from A9 go to the A10 motherboard through connector P1 and to the A4 sweeper board through connector P2 as shown in Figure 8-87.

Each regulator circuit employs a three-pin, monolithic regulator (U1 thru U8) that has internal overcurrent and over-temperature protection. To allow for more efficient cooling, the 5 volt regulator, U2, has a T03 case and is mounted on a separate heatsink along with its bridge rectifier. All the other regulators use the T0220 case and are mounted on an aluminum heatsink that is bolted along one edge of the PCB.

b. Polyswitch. The polyswitches (RT1 thru RT7) are temperature dependent resistors used as solid state fuses. Polyswitches (except at the +5V circuit) are used to ensure that the regulated outputs are short-circuit protected in case of an equipment failure. They also ensure that failure of the power supply does not cause damage to other circuits within the instrument. A discussion follows.

When the maximum current rating of the polyswitch is exceeded, internal heating causes it to increase in resistance very rapidly by several orders of magnitude. The resultant low current/high voltage condition of the device causes only a small amount of power to be dissipated by the polyswitch. This small power level keeps the device in a high impedance state, which results in only a very small amount of power being dissipated by the failure that caused the condition.

The polyswitch is reset by switching the line power OFF for a approximately ten minutes to allow the device to cool.

c. Regulator Circuits. The linear regulator circuits provide required supply voltages to the instrument. Table 8-14 shows these voltages plus typical and maximum current ratings. Since all the regulator circuits are very similar, only one is fully described. Major differences in the other sections, however, are detailed below.

The 12 Volt supply for the video monitor is derived from the 15 volt RMS winding on the transformer and is taken to bridge rectifier CR18 through polyswitch RT2.

Table 8-14. Power Supply Outputs

REGULATOR	DC VOLTAGE	TYPICAL DC CURRENT	MAXIMUM DC CURRENT	USED MAINLY BY
U1	+12 Volts	1.0 Amps	1.4 Amps	Video monitor
U2	+ 5 Volts	2.8 Amps	3.4 Amps	All logic
U3	-18 Volts	350 mA	530 mA	YIG tuning
U4	+15 Volts	125 mA	250 mA	Signal Channel
U5	-15 Volts	100 mA	250 mA	Signal Channel
U6	+18 Volts	500 mA	640 mA	Sweeper Board
U7	-18 Volts	300 mA	640 mA	Sweeper Board
U8	+25 Volts	150 mA	260 mA	Switched Attenuator

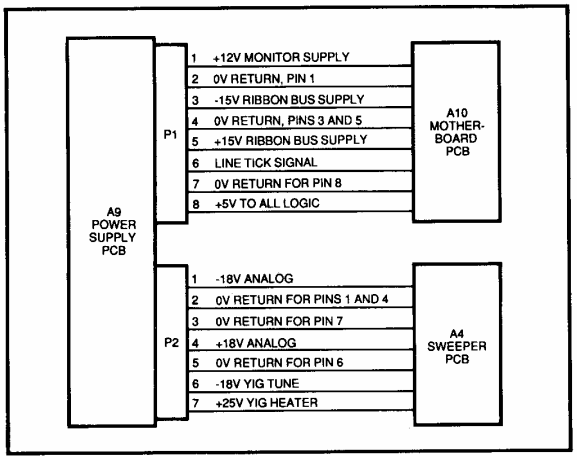


Figure 8-87. Regulated Outputs

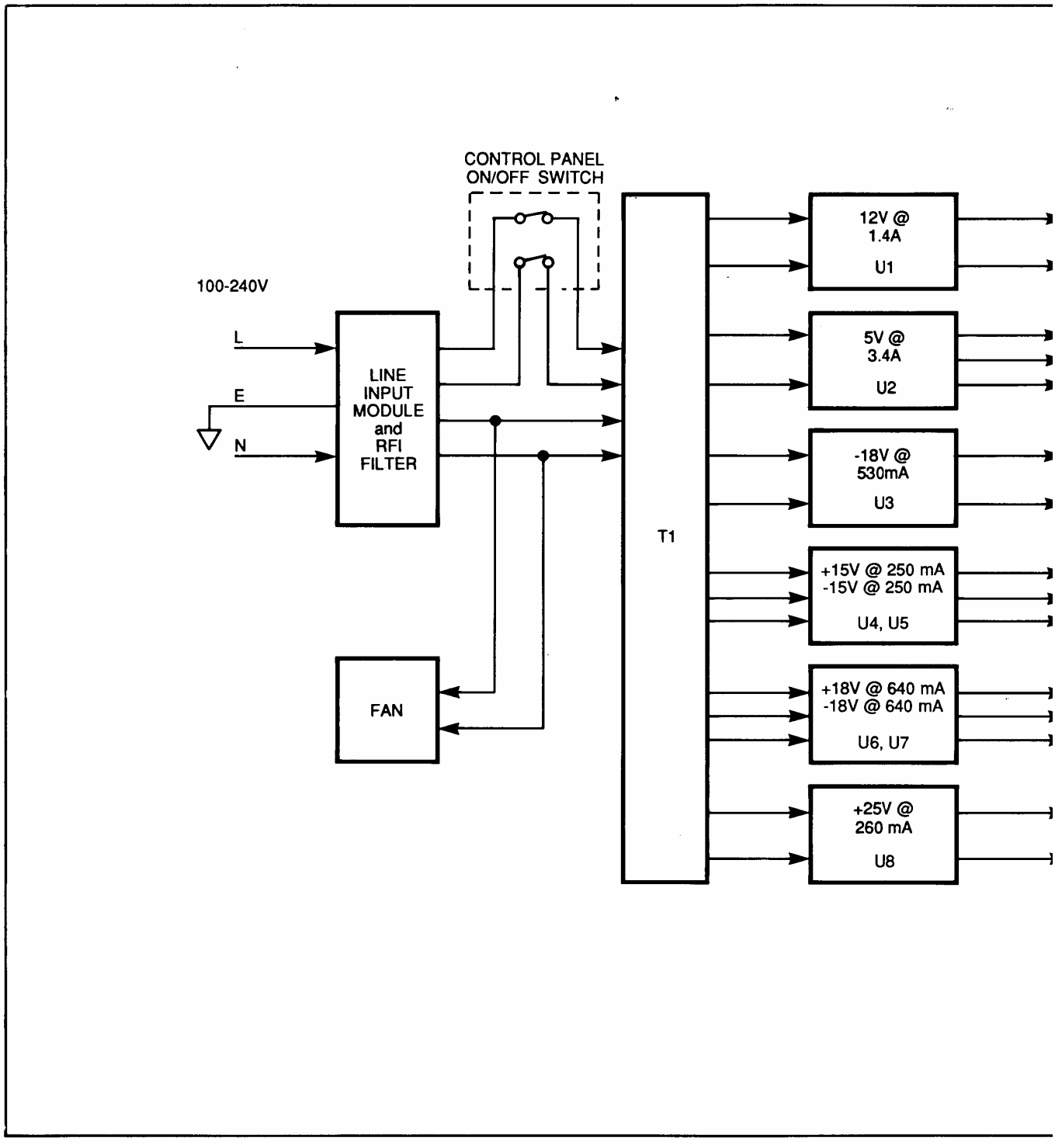
Rectified voltage from CR18 charges reservoir capacitor C1. A safety discharge path for this circuit is provided by resistor R1. The monolithic regulator, U1, produces the required output voltage of +12V. This regulator is protected from the output line by hold-up diode CR9. Final decoupling for the regulator is provided by capacitors C2 and C3.

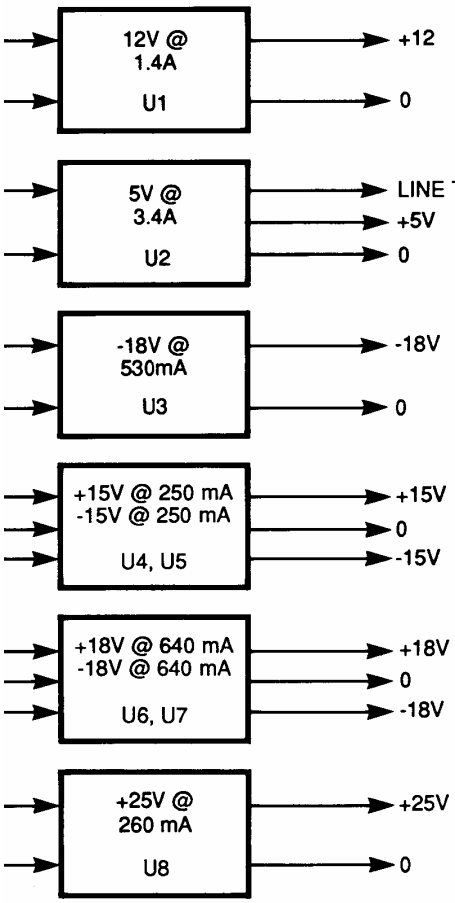
All of the supply rails follow the same pattern. The +/-15V and the +/-18V rails, however, have additional diodes across their outputs to protect them from reverse biasing.

The +25V rail is regulated by a 15V monolithic regulator, U8, that has its reference-ground terminal biased to +10V by CR16. This biasing is through R9.

d. PSU ON/OFF LED Indicator. The power supply ON/OFF indicator is provided by a resistor and LED indicator across the output of the +5V rail. These components are located on the component side of the PCB.

e. Line Trigger. The line trigger is a logic level signal output that is derived from the ac line. It is used by the A6 microprocessor PCB to perform real time events and timings. The trigger output is formed by CR24, R11, R12, C26, and C29.


CONTROL PANEL
ON/OFF SWITCH
100-240V
L
E
N
LINE
INPUT
MODULE
and
RFI
FILTER
FAN
T1
12V @
1.4A
U1
5V @
3.4A
U2
-18V @
530mA
U3
+15V @ 250 mA
-15V @ 250 mA
U4, U5
+18V @ 640 mA
-18V @ 640 mA
U6, U7
+25V @
260 mA
U8



VOLTAGE	CURRENT	LOAD	WATTAGE
+12V	1.4A	10 Ω	15W
+5V	3.4A	1.5 Ω	20W
-18V	530mA	36 Ω	10W
+15V	250mA	60 Ω	5W
-15V	250mA	60 Ω	5W
+18V	640mA	36 Ω	10W
-18V	640mA	36 Ω	10W
+25V	260mA	100 Ω	7W

Figure 8-88. A9 Power Supply Block Diagram

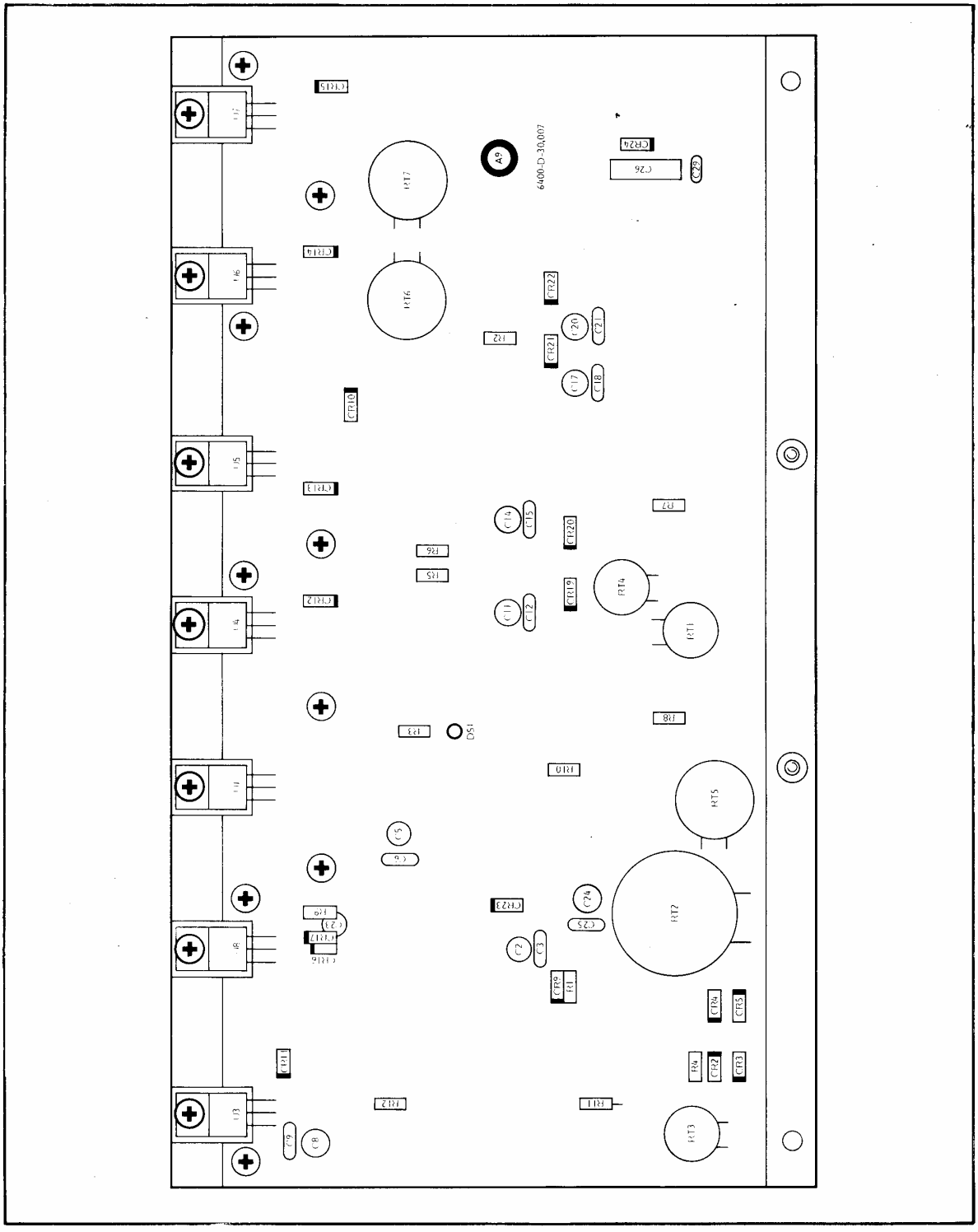
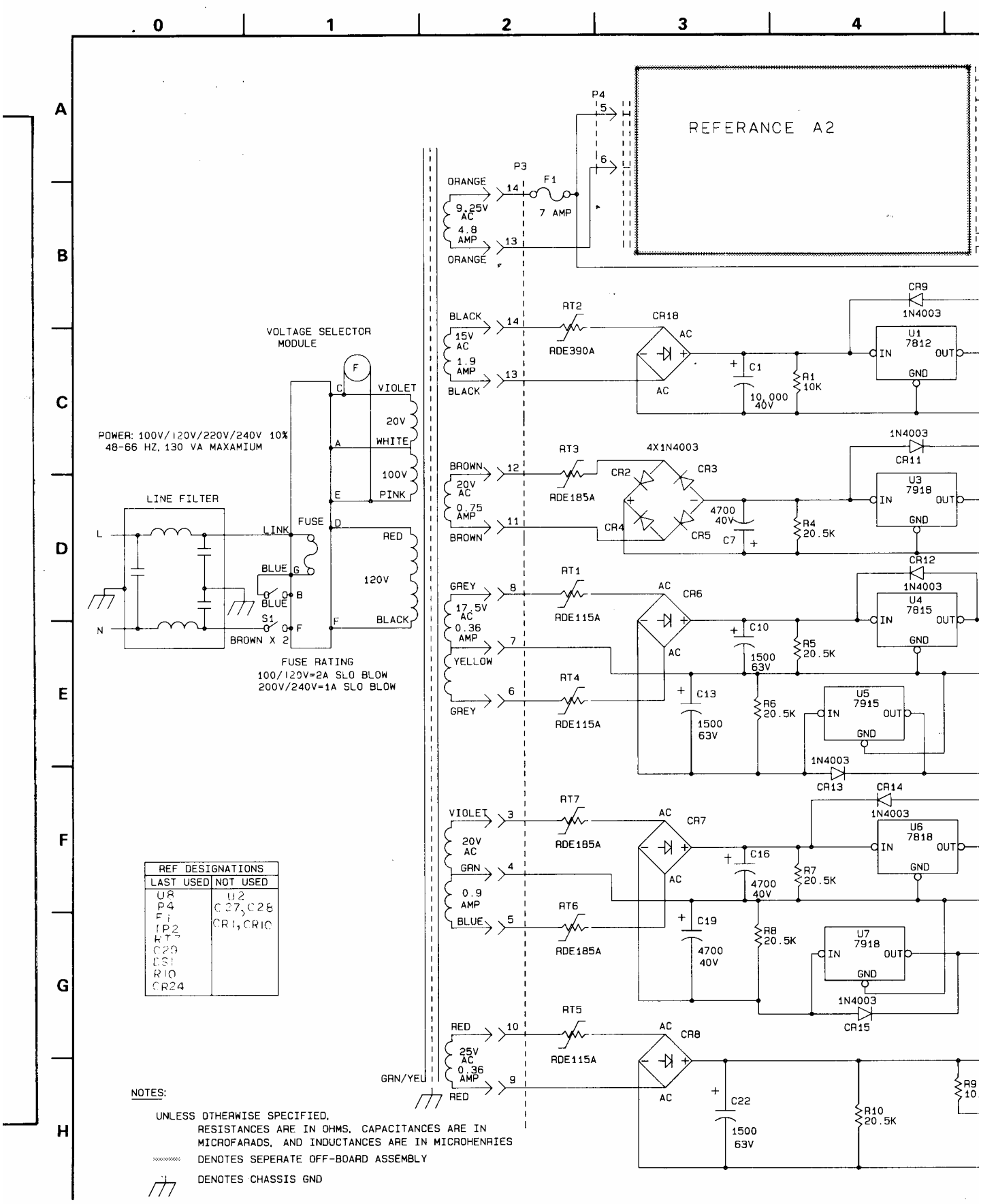
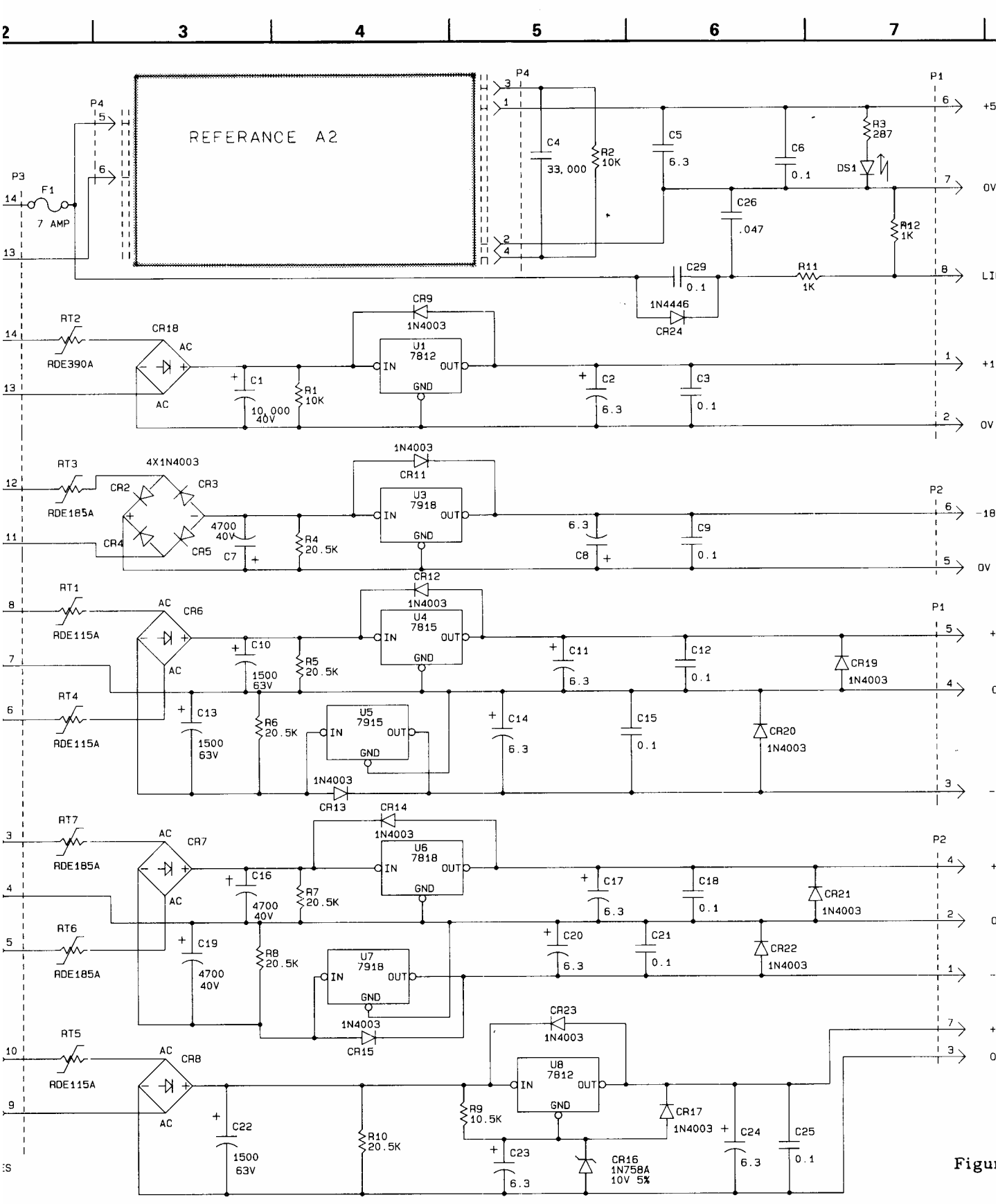


Figure 8-89. A9 PCB Parts Locator Diagram


REFERANCE A2
P4
P3
F1
7 AMP
ORANGE
9.25V AC
4.8 AMP
VOLTAGE SELECTOR MODULE
POWER: 100V/120V/220V/240V 10%
48-66 HZ. 130 VA MAXAMIUM
LINE FILTER
FUSE
LINK
VIOLET
20V
WHITE
100V
PINK
RED
120V
BLACK
BLUE
BROWN X 2
FUSE RATING
100/120V=2A SLO BLOW
200V/240V=1A SLO BLOW
BLACK
15V AC
1.9 AMP
RT2
RDE390A
CR18
C1
10,000 40V
R1 10K
CR9
1N4003
U1 7812
IN
OUT
GND
BROWN
20V AC
0.75 AMP
RT3
RDE185A
4X1N4003
CR2
CR3
CR4
CR5
4700 40V
C7
R4 20.5K
CR11
U3 7918
GREY
17.5V AC
0.36 AMP
YELLOW
RT1
RDE115A
CR6
C10
1500 63V
R5 20.5K
CR12
U4 7815
RT4
C13
R6 20.5K
U5 7915
CR13
VIOLET
20V AC
GRN
0.9 AMP
BLUE
RT7
CR7
C16
4700 40V
R7 20.5K
CR14
U6 7818
RT6
C19
R8 20.5K
U7 7918
CR15
RED
25V AC
0.36 AMP
RT5
CR8
C22
1500 63V
R10 20.5K
R9 10
GRN/YEL
REF DESIGNATIONS
LAST USED
NOT USED
U8
P4
F1
TP2
RT5
C29
DS1
R10
CR24
U2
C27,C28
CR1,CR10
NOTES:
UNLESS OTHERWISE SPECIFIED,
RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS, AND INDUCTANCES ARE IN MICROHENRIES
DENOTES SEPERATE OFF-BOARD ASSEMBLY
DENOTES CHASSIS GND


2
3
4
5
6
7
REFERANCE A2
P4
P3
P1
P2
F1
7 AMP
C4
33,000
R2
10K
C5
6.3
C6
0.1
R3
287
DS1
C26
.047
R12
1K
C29
0.1
R11
1K
1N4446
CR24
+5
0V
LI
RT2
RDE390A
CR18
AC
C1
10,000
40V
R1
10K
CR9
1N4003
U1
7812
IN
OUT
GND
C2
6.3
C3
0.1
+1
RT3
RDE185A
4X1N4003
CR2
CR3
CR4
CR5
C7
4700
40V
R4
20.5K
CR11
U3
7918
C8
C9
-18
RT1
RDE115A
CR6
C10
1500
63V
R5
20.5K
CR12
U4
7815
C11
C12
CR19
1N4003
RT4
C13
R6
20.5K
U5
7915
C14
C15
CR20
CR13
CR14
RT7
CR7
C16
4700
40V
R7
20.5K
U6
7818
C17
C18
CR21
RT6
C19
R8
20.5K
U7
7918
C20
C21
CR22
CR15
CR23
RT5
CR8
C22
1500
63V
R10
20.5K
R9
10.5K
U8
7812
CR17
C24
C25
C23
6.3
CR16
1N758A
10V 5%

Figu

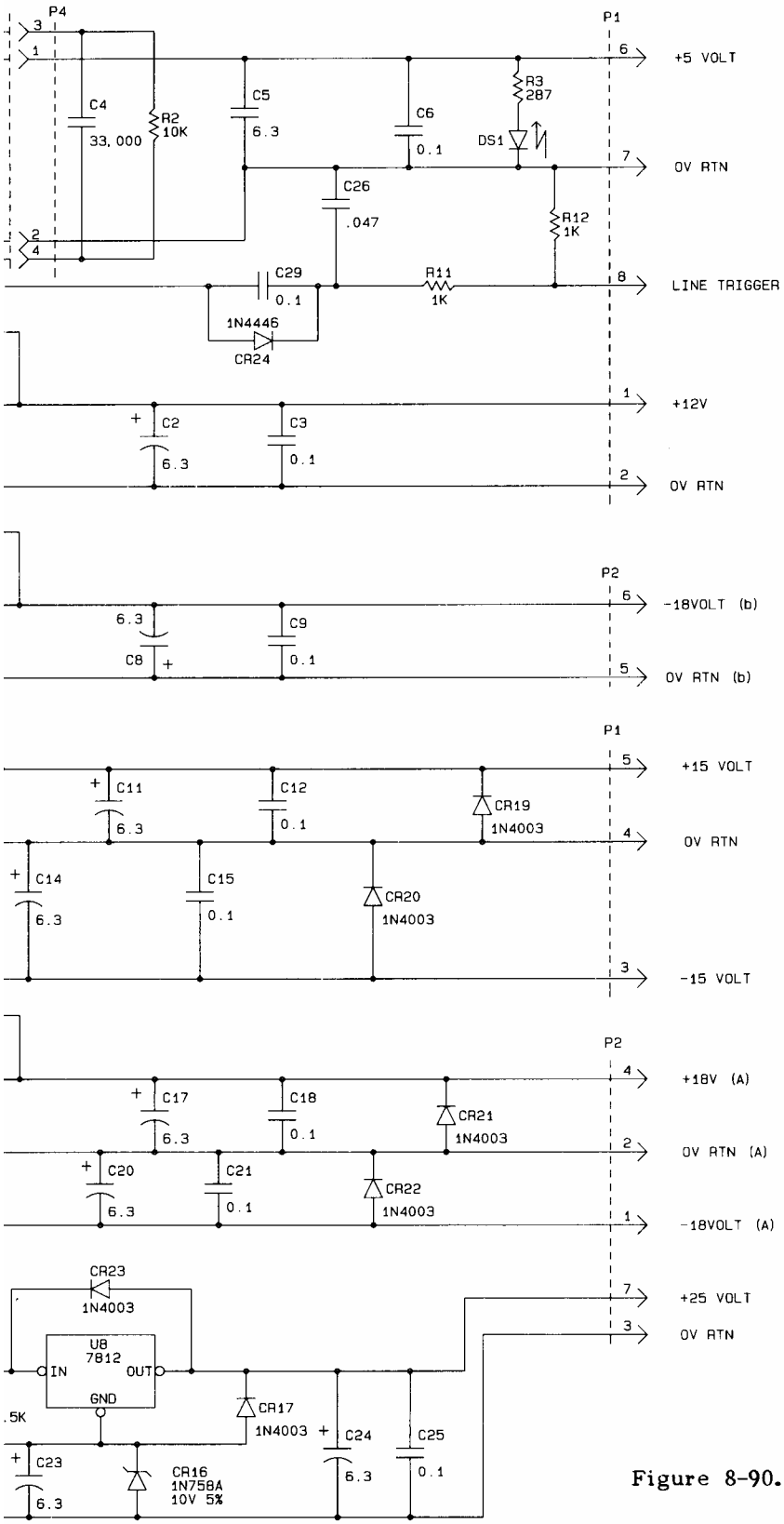


Figure 8-90. A9 Power Supply Schematic

8-7.10 A10 Motherboard PCB

The A10 Motherboard provides the medium for connecting the digital PCBs to each other, to the rest of the assemblies, and to the outside world. Tables 8-15 thru 8-23 contain each different connector's pin numbers and the associated signal identification.

The two circuits on this PCB are the tick signal squaring circuit and the hard copy circuit. The tick signal squaring circuit is shown in Figure 8-91. The printer circuit is shown in Figure 8-92. The parts locator diagram and schematic are shown in Figures 8-93 and 8-94.

a. Connectors

1. Connector P1. Connector P1 goes to the ribbon bus that connects the A6 CPU PCB to the A3 Signal Channel, A1 control panel, and A4 Sweeper PCBs. Marker information is derived from the A4 PCB. Power required by the A1 control panel and the A3 signal channel PCBs is also carried over this bus.

2. Connector P2. The A8 GPIB option communicates and receives power through connector P2. A high frequency clock line runs through this ribbon cable. To minimize distortion, this clock line is sandwiched between two ground wires.

3. Connector P3. Connector P3 takes the composite video to the rear panel BNC connector.

Table 8-15. Connector P1

Pin No.	Signal Ident.	Pin No.	Signal Ident.
1	n/c	18	D4
2	n/c	19	D3
3	-15V	20	D2
4	$0V_{analog}$	21	D1
5	+15V	22	D0
6	$0V_{digital}$	23	A7
7	+5V	24	A6
8	$\overline{INT_6}$	25	A5
9	$\overline{INT_5}$	26	A4
10	$\overline{INT_4}$	27	A3
11	$\overline{INT_3}$	28	A2
12	n/c	29	A1
13	$\overline{PSB}$	30	A0
14	IO/$\overline{M}$	31	$\overline{IOSEL_3}$
15	D7	32	$\overline{IOSEL_2}$
16	D6	33	$\overline{IOSEL_1}$
17	D5	34	$\overline{IOSEL_0}$

Table 8-16. Connector P2

Pin No.	Signal Ident.	Pin No.	Signal Ident.
1	D0	11	A2
2	D1	12	A3
3	D2	13	$\overline{RD}$
4	D3	14	$\overline{IOSEL_5}$
5	D4	15	$\overline{WR}$
6	D5	16	+5V
7	D6	17	$\overline{INT_2}$
8	D7	18	0V
9	A0	19	CLK
10	A1	20	0V

Table 8-17. Connector P3

Pin No.	Signal Ident.
1	Composite Video Output
2	Video Ground

4. Connector P4. Connector P4 interfaces with the printer.

Table 8-18. Connector P4 Centronics Connector

Pin No.	Signal Ident.	Pin No.	Signal Ident.
1	$\overline{STB}$	19	0V
2	D0	20	0V
3	D1	21	0V
4	D2	22	0V
5	D3	23	0V
6	D4	24	0V
7	D5	25	0V
8	D6	26	0V
9	D7	27	0V
10	$\overline{ACK}$	28	0V
11	BUSY	29	0V
12	PAP OUT	30	0V
13	SEL	31	$\overline{INIT}$
14	--	32	n/c
15	--	33	0V
16	0V	34	n/c
17	0V	35	n/c
18		36	n/c

Table 8-19. Connector P4 Motherboard

Pin No.	Signal Ident.	Pin No.	Signal Ident.
1	$\overline{STB}$	18	0V
2	0V	19	$\overline{ACK}$
3	D0	20	0V
4	0V	21	BUSY
5	D1	22	0V
6	0V	23	PAP OUT
7	D2	24	0V
8	0V	25	SEL
9	D3	26	$\overline{INIT}$
10	0V	27	n/c
11	D4	28	n/c
12	0V	29	n/c
13	D5	30	0V
14	0V	31	0V
15	D6	32	n/c
16	0V	33	0V
17	D7	34	n/c

5. Connector P5. Connector P5 brings power from A9 to the other PCBs, the ribbon bus, and the CRT. P5 also carries the line tick signal. The A4 PCB however, receives power to A4, P6 from A9, P2.

Table 8-20. Connector P5

Pin No.	Signal Ident.
1	+12V Monitor Supply
2	0V return PIN 1
3	-15V Ribbon Bus supply
4	0V return for PINs 3 and 5
5	+15V Ribbon Bus supply
6	Line tick signal
7	0V return for PIN 8
8	+5V supply to all logic

6. Connector P6. P6 makes the connection between the intensity control potentiometer on A11 to A10.

Table 8-21. Connector P6

Pin No.	Signal Ident.
1	Video Ground
2	Return from the Control Panel
3	Send to the Control Panel
4	Unallocated

7. Connector P7. Connector P7 carries power plus video and synchronization signals to the CRT.

Table 8-22. Connector P7 Video Monitor

Pin No.	Signal Ident.
1	HSYNC
2	Screen
3	VIDEO
4	Screen
5	/VSYNC
6	+12 Volt Supply

8. Connector P8. Connector P8 is the central processor unit (A6) PCB edge connector.

9. Connector P9. Connector P9 is the Graphic Display Processor (A7) PCB edge connector.

Table 8-23. Connector P8

(Circuit side of the PCB)		(Component side of the PCB)	
Pin No.	Signal Ident.	Pin No.	Signal Ident.
A	D0	1	D1
B	D2	2	D3
C	D4	3	D5
D	D6	4	D7
E	$\overline{RD}$	5	$\overline{WR}$
F	A0	6	A1
H	A2	7	A3
J	A4	8	A5
K	A6	9	A7
L	$\overline{PSB}$	10	IO/M
M	CLOCK	11	n/c
N	n/c	12	n/c
P	n/c	13	n/c
R	+5V	14	+5V
S	0V	15	0V
T	$\overline{IOSEL_0}$	16	$\overline{IOSEL_1}$
U	$\overline{IOSEL_2}$	17	$\overline{IOSEL_3}$
V	$\overline{IOSEL_4}$	18	$\overline{IOSEL_5}$
W	$\overline{IOSEL_6}$	19	$\overline{IOSEL_7}$
X	$\overline{INT_7}$	20	$\overline{INT_6}$
Y	$\overline{INT_5}$	21	$\overline{INT_4}$
Z	$\overline{INT_3}$	22	$\overline{INT_2}$
AA	$\overline{INT_1}$	23	$\overline{INT_0}$
BB	n/c	24	n/c
CC	n/c	25	$\overline{VSYNC}$
DD	n/c	26	-15V
EE	PLLCONT	27	+15V
FF	$\overline{RESET}$	28	TICK

Table 8-24. Connector P9

(Circuit side of the PCB)		(Component side of the PCB)	
Pin No.	SIGNAL Ident.	Pin No.	Signal Ident.
A	D0	1	D1
B	D2	2	D3
C	D4	3	D5
D	D6	4	D7
E	$\overline{RD}$	5	$\overline{WR}$
F	A0	6	--
H	n/c	7	--
J	n/c	8	--
K	n/c	9	--
L	n/c	10	--
M	n/c	11	--
N	n/c	12	--
P	n/c	13	--
R	+5V	14	+5V
S	0V	15	0V
T	n/c	16	--
U	n/c	17	--
V	n/c	18	--
W	$\overline{IOSEL_6}$	19	--
X	n/c	20	--
Y	n/c	21	--
Z	VSCRN	22	VSCRN
AA	COMPVID	23	VSCRN
BB	$\overline{VSYNC}$	24	VSCRN
CC	VSCRN	25	VIDEO
DD	HSYNC	26	VSCRN
EE	n/c	27	--
FF	VCOIN	28	--

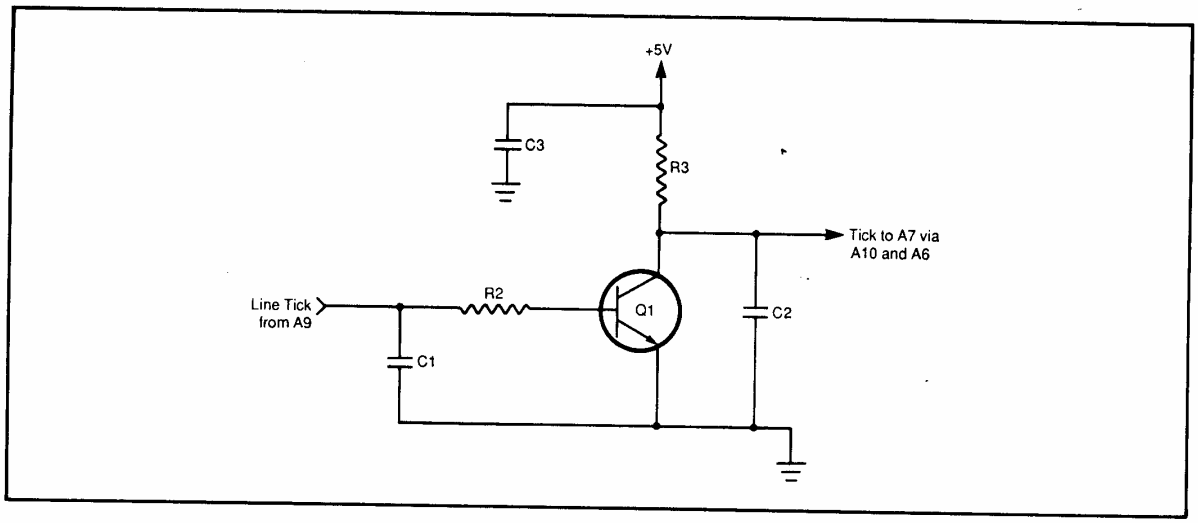


Figure 8-91. Tick Signal Squaring Circuit

b. Circuits

1. Line Tick Circuit. The line tick is a synchronization pulse that stabilizes the display on the CRT. This pulse comes from the A9 PCB and goes to the A7 PCB via the A10 and A6 PCBs. The line tick circuit is shown in Figure 8-91.

   The line tick is squared by Q1. A logic level signal is fed to the base of Q1 through R2. The signal reappears at the collector of Q1 inverted, squared off, and at the same TTL logic level. Capacitors C1 and C2 prevent any fast edges that might interfere with the timing opertion.

2. Printer Control Circuit. This circuit controls the several operations needed to print data. The operations are:

   (a) Holding the data until the printer is ready to accept it.

   (b) Reading the printer's acknowledging signal that the data has been accepted.

   (c) Reading any status signals from the printer; such as, printer busy, printer out of paper, printer selected.

   (d) Reseting the printer to its Power ON default settings.

   The printer circuit consists of ICs U1 thru U3 and associated components. A simplified schematic is shown in Figure 8-92, and the schematic is shown in Figure 8-94. Refer to the simplified schematic for the following discussion.

   The controlling chip in this circuit is decoder U4. The output lines on this IC generate logic signals that perform the following sequential actions:

   (a) The Y_0 output clocks the data through latch U2 and out to the printer.

   (b) The Y_1 output sends a strobe pulse ($\overline{STB}$) to the printer that tells it valid data is on the line.

(c) The Y_2 output clears the Acknowledge flip-flop (ACK FF), A3, so that it is ready to respond to the printer's acknowledging signal ($\overline{ACK}$) that the data has been received.

(d) The Y_3 output enables the status latch (U1) to read the four printer status lines: $\overline{ACK}$, BUSY, PE, and SELECT.

(e) The Y_4 output presets the RESET flip flop, U3, for an inactive, logic-high Q output.

(f) The Y_5 output clears the RESET flip flop for an active-state, logic-low Q output. This output sets the $\overline{RESET}$ output line to its active-low state. The $\overline{RESET}$ line resets the printer.

The operation of U4 is as follows:

(a) Select output Y_0. Thisl output is selected when the six input lines have the logic states shown below:
(1) A0-A2: low (I/0 port: 58H)
(2) A3: high
(3) $\overline{PSB}$: low
(4) $\overline{IOSEL5}$: low

Approximately 1 µS after having been selected, the $\overline{PSB}$ line returns to its inactive HIGH state and deselects the Y_0 output. This output then goes HIGH and clocks the data through latch U2.

(b) Select output Y_1. Same as (a) above, except the A0-A2 logic status is:
(1) A0: high
(2) A1: low
(3) A2: low (I/O port: 59H).

The Y_1 output provides the 1 µS active low strobe pulse ($\overline{PSB}$) to the printer.

(c) Select output Y_2. Same as (a) above, except the A0-A2 logic status is:
(1) A0: low
(2) A1: high
(3) A2: low (I/O port: 5AH).

The Y_2 output clears the Acknowledge FF.

(d) Select output Y_3. Same as (a) above, except the A0-A2 logic status is:
(1) A0: high
(2) A1: high
(3) A2: low (I/O port: 5BH).

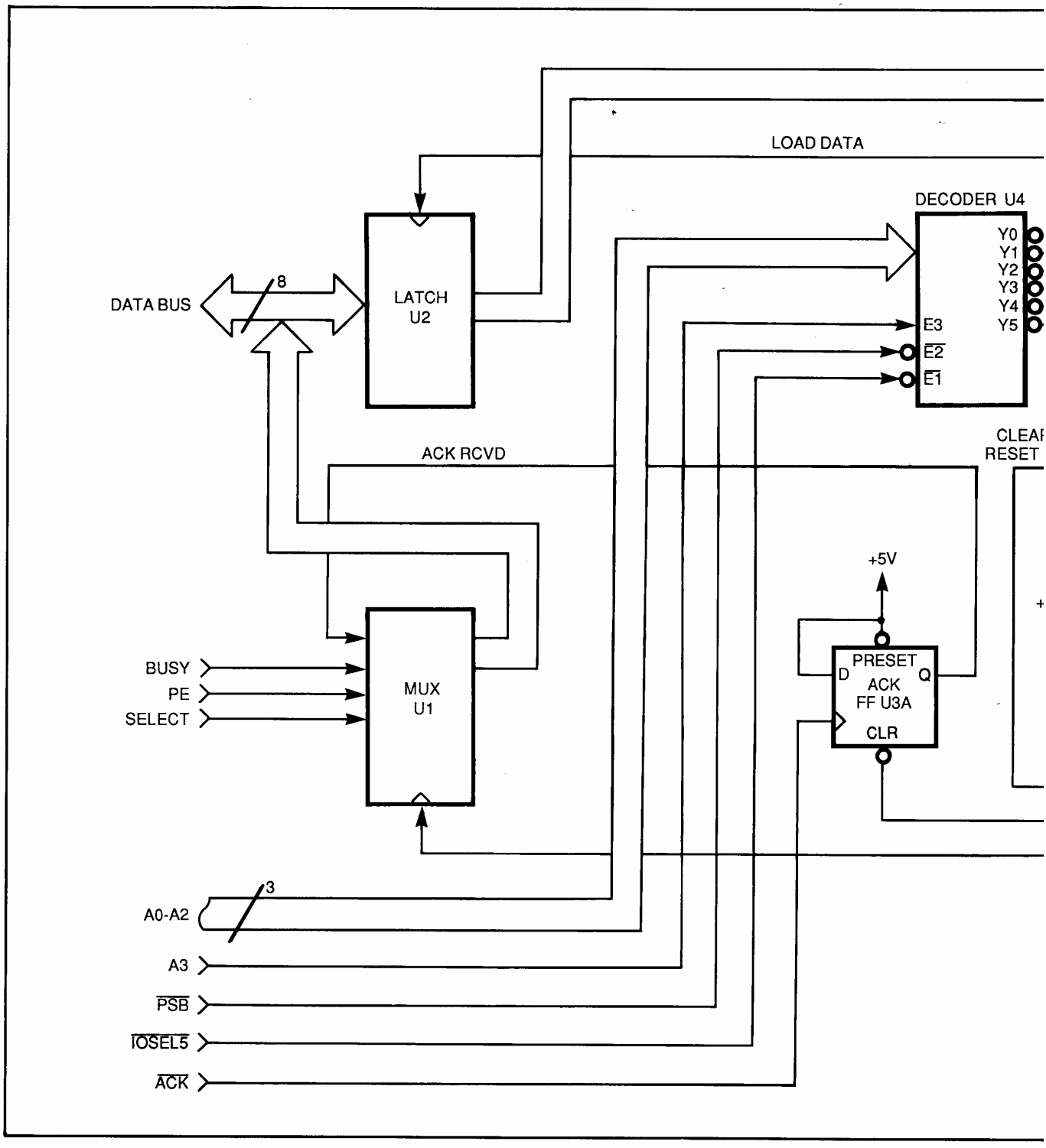
The Y_3 output enables the status latch, U1.

(e) Select output Y_4. Same as (a) above, except the A0-A2 logic status is:
(1) A0: low
(2) A1: low
(3) A2: high (I/O port: 5CH).

The Y_4 output presets the RESET FF, U3B.

(f) Select output Y_5. Same as (a) above, except the A0-A2 logic status is:
(1) A0: high
(2) A1: low
(3) A2: high (I/O port: 5DH).

The Y_5 output clears the RESET FF, U3B.


LOAD DATA
DECODER U4
Y0
Y1
Y2
Y3
Y4
Y5
E3
E2
E1
DATA BUS
8
LATCH
U2
ACK RCVD
CLEAR
RESET
+5V
PRESET
D
Q
ACK
FF U3A
CLR
BUSY
PE
SELECT
MUX
U1
3
A0-A2
A3
PSB
IOSEL5
ACK

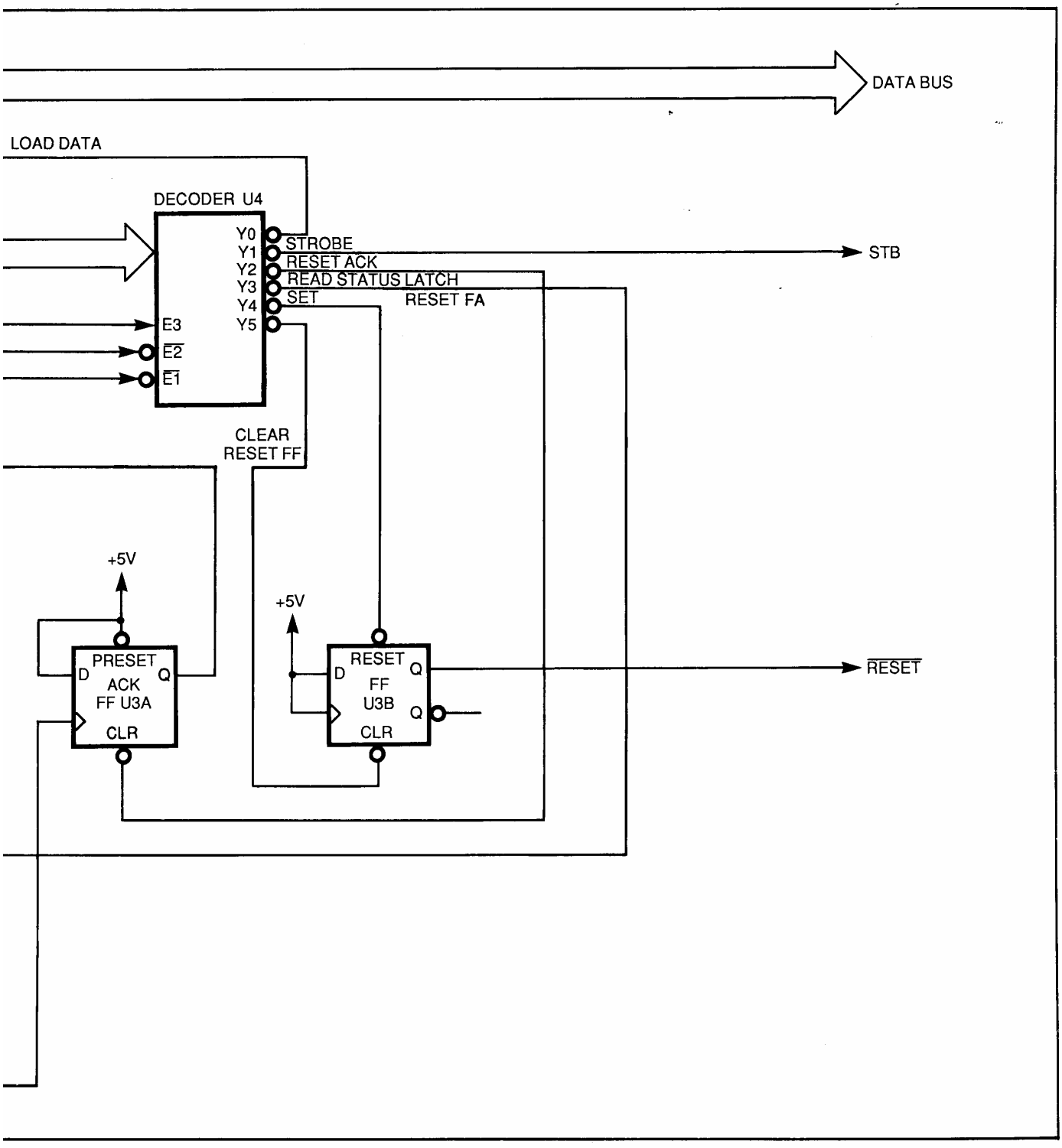


Figure 8-92. Printer Circuit Block Diagram

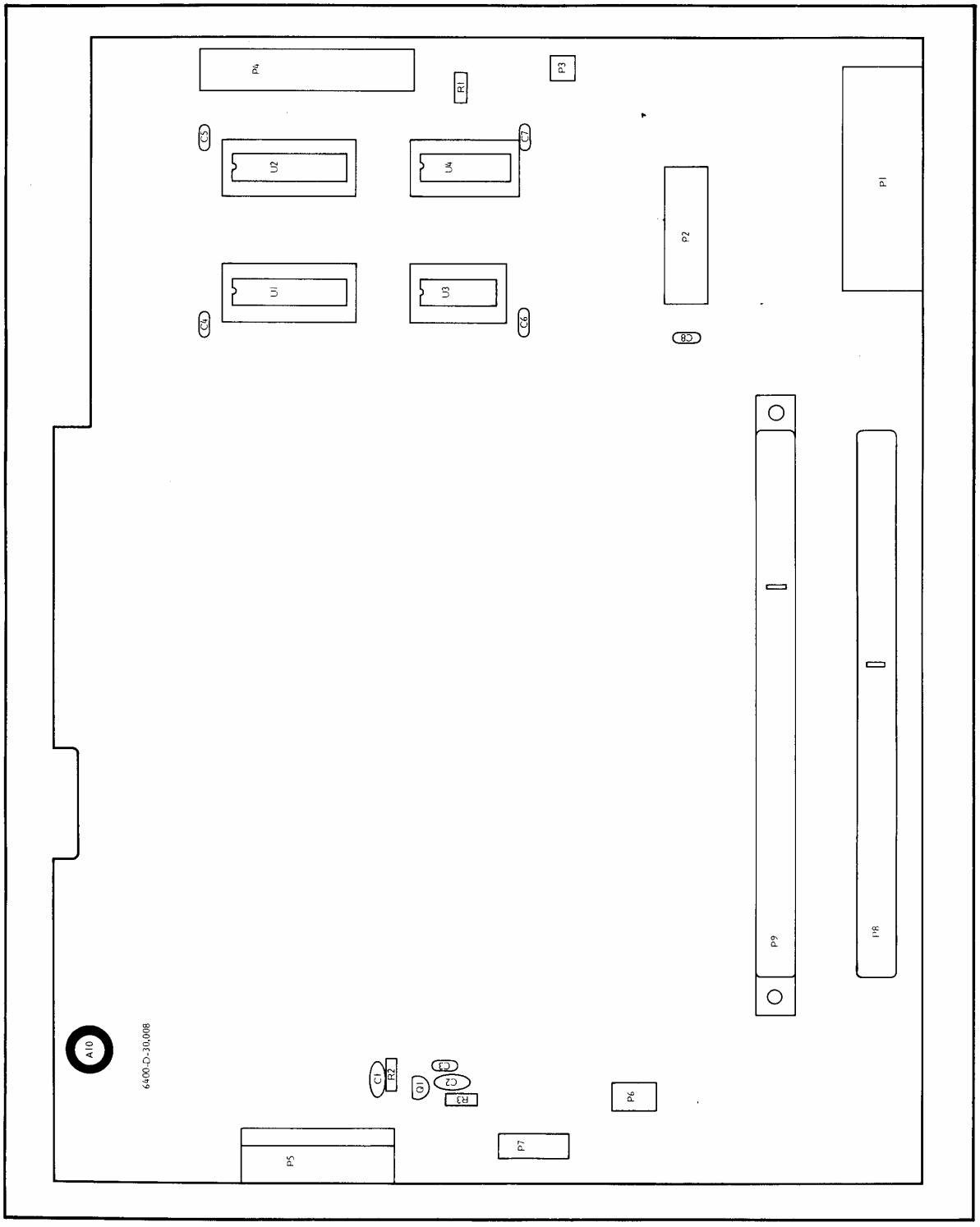
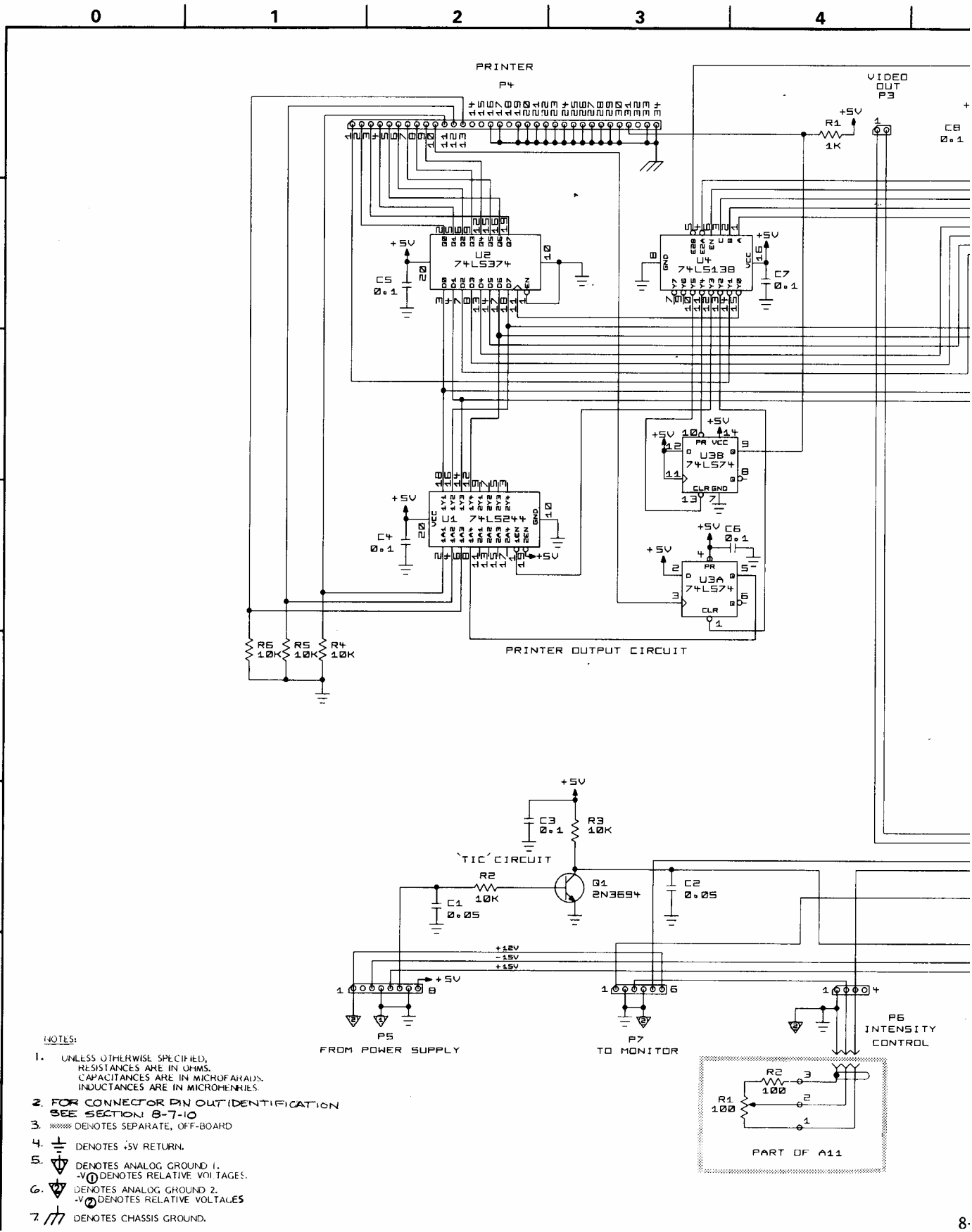


Figure 8-93. A10 PCB Parts Locator Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN MICROFARADS. INDUCTANCES ARE IN MICROHENRIES.
2. FOR CONNECTOR PIN OUT IDENTIFICATION SEE SECTION 8-7-10
3. DENOTES SEPARATE, OFF-BOARD
4. DENOTES +5V RETURN.
5. DENOTES ANALOG GROUND 1. -V① DENOTES RELATIVE VOLTAGES.
6. DENOTES ANALOG GROUND 2. -V② DENOTES RELATIVE VOLTAGES
7. DENOTES CHASSIS GROUND.

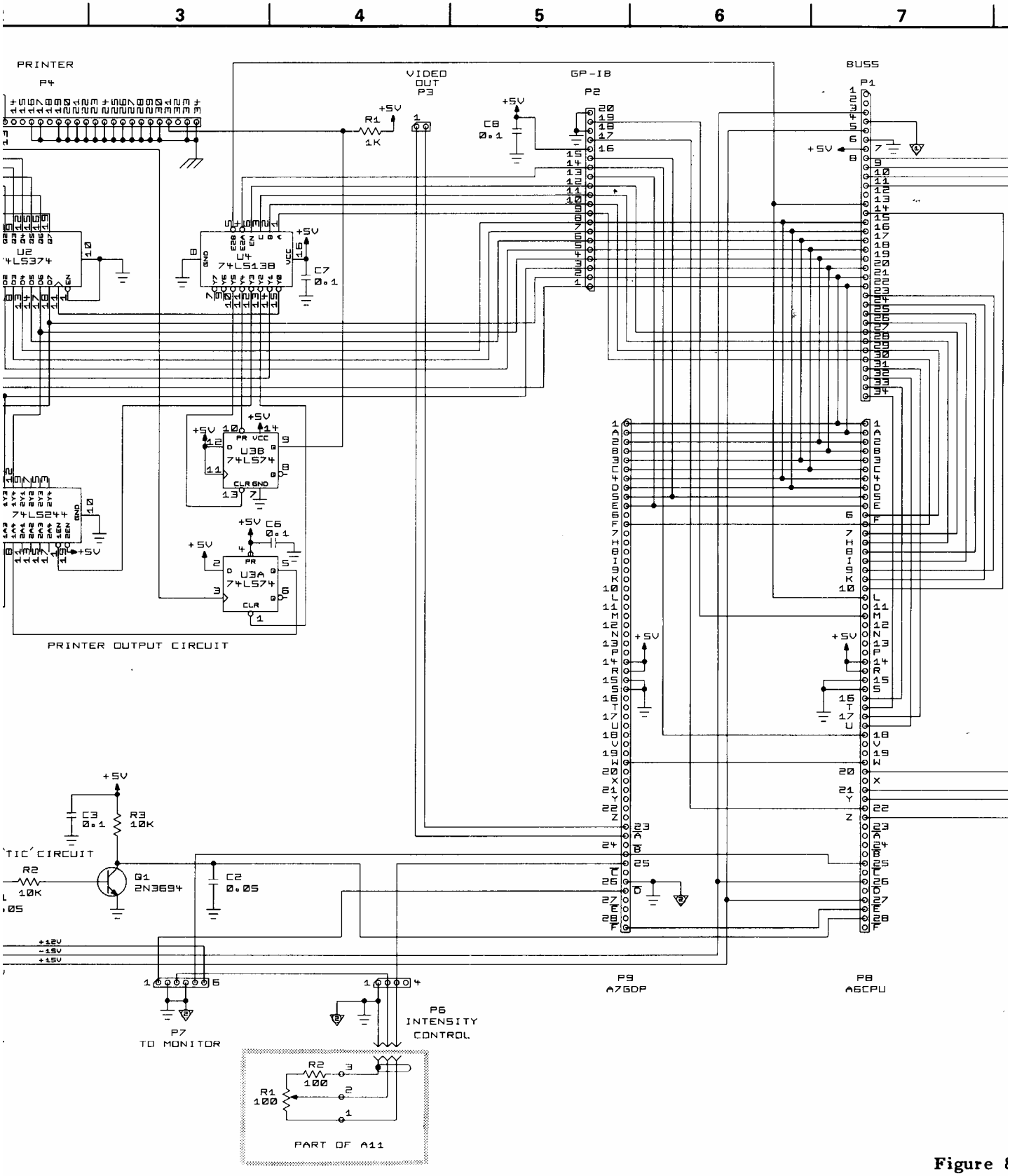

3
4
5
6
7
PRINTER
P4
VIDEO
OUT
P3
GP-IB
P2
BUSS
P1
+5V
R1
1K
C8
0.1
U2
74LS374
U4
74LS138
C7
0.1
74LS244
U3B
74LS74
U3A
74LS74
C6
0.1
PRINTER OUTPUT CIRCUIT
C3
0.1
R3
10K
R2
10K
Q1
2N3694
C2
0.05
+12V
-15V
+15V
P9
A7GDP
P8
A6CPU
P7
TO MONITOR
P6
INTENSITY
CONTROL
R2
100
R1
100
PART OF A11

Figure 8

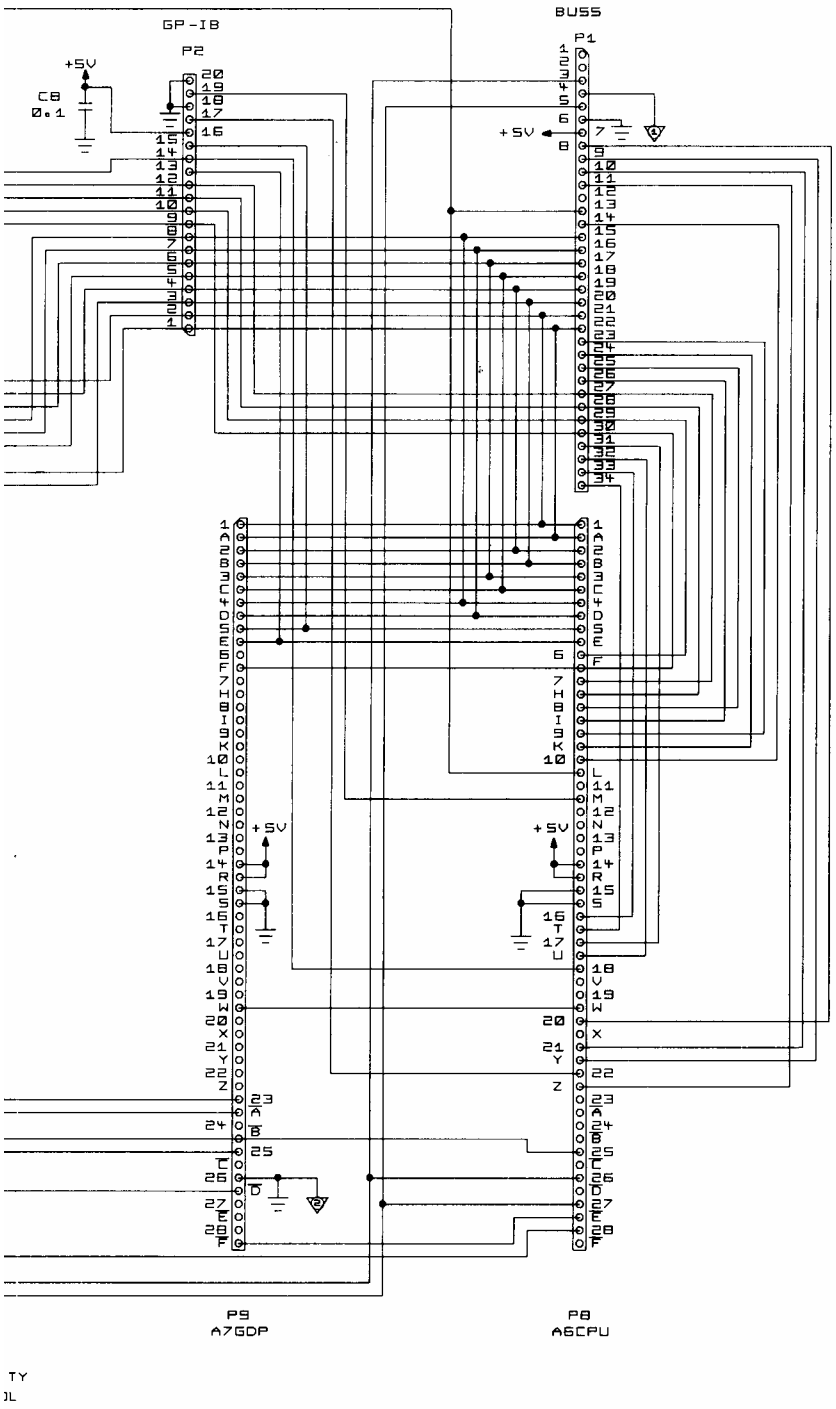


Figure 8-94. A10 Motherboard Schematic

8-7.11 A11 Control Panel PCB

The A11 Subsidiary Control Panel PCB contains the switches for MENU SELECT, MENU UP/DOWN, and GRATICULE ON/OFF. The video intensity control is also mounted on this PCB. The A11 block and parts locator diagrams are shown in Figures 8-96 and 8-97 respectively. The A11 schematic is shown with the A1 schematic in Figure 8-28.

a. Switches. The A11 PCB switches--MENU SELECT, MENU UP/DOWN, and GRATICULE ON/OFF--are connected into the control panel matrix via Connector P1. Figure 8-95 shows the A11 switch matrix lines.

The GRATICULE ON/OFF is operated by switch S1; the MENU UP/DOWN by switch S2; and, MENU SELECT by switch S3. Switch S2 is a center-biased, on-off-on, single pole, double throw, rocker switch. Diodes CR1 thru CR4 provide signal routing, which allows S2 to operate as two normal, double pole, single throw buttons.

b. Intensity Control. The intensity control varies the video level to the monitor. This control, located in the video signal path, has less than 5V of signal. The intensity potentiometer consists of R1 and R2. Resistor R2 ensures that the display cannot be turned all the way down. Consequently, it is impossible to have a completely blank screen.

The intensity control connection to the A10 Motherboard is through Connector S1. The pin numbers and connections are shown below.

S1 PIN	Cable	Connected to:
1	screen	Ground
2	black	Video return to CRT
3	red	Video send from GDP

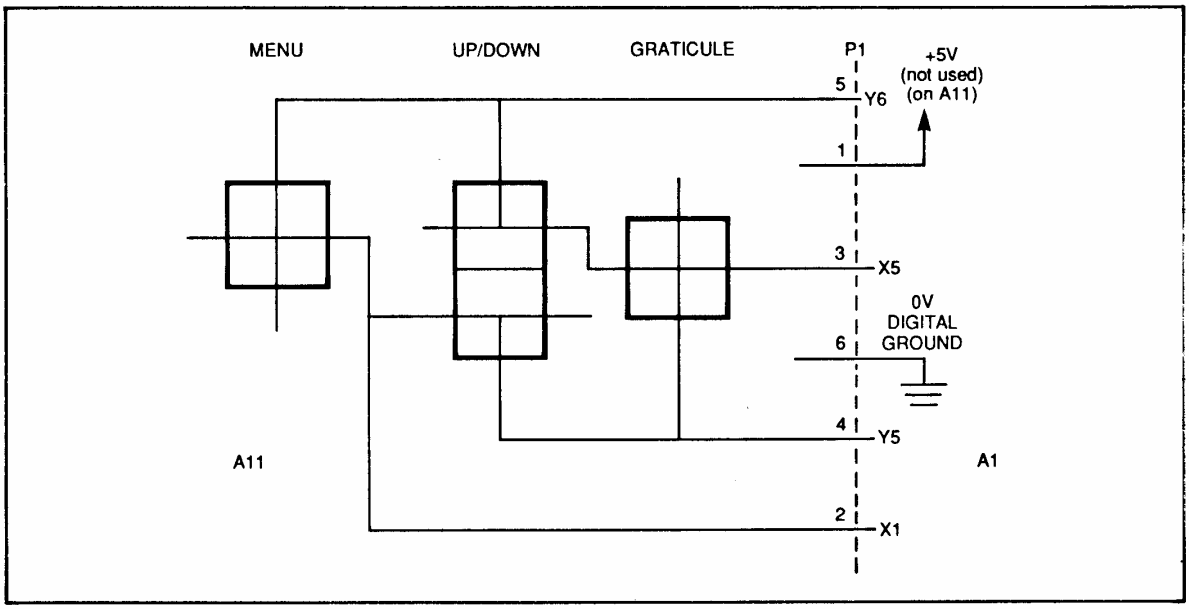


Figure 8-95. Switch Matrix Lines

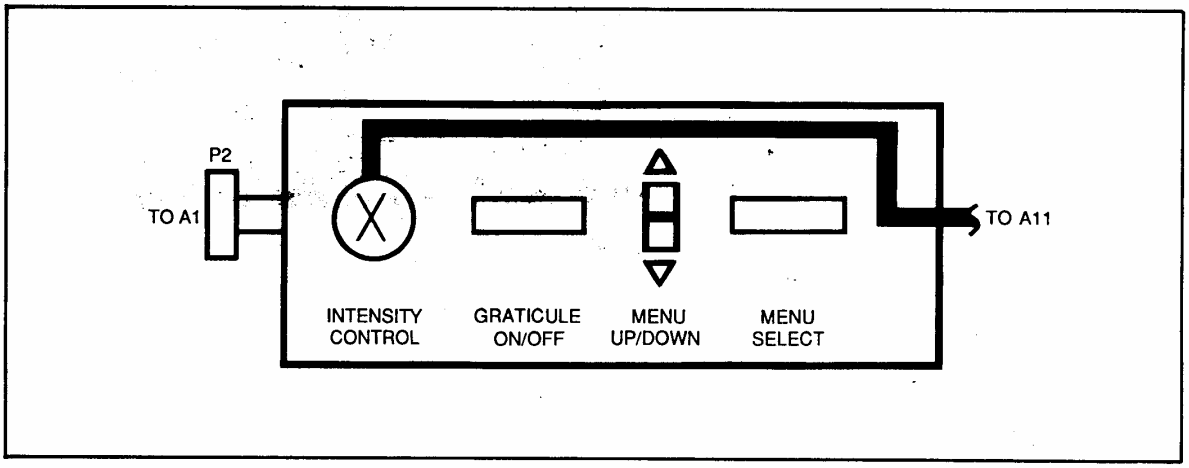


Figure 8-96. A11 Subsidiary Control Panel Block Diagram

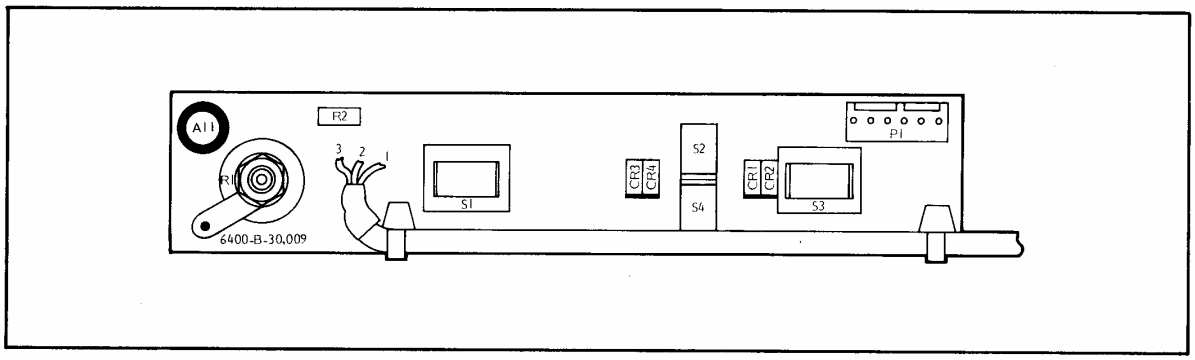


Figure 8-97. A11 PCB Parts Locator Diagram